ReRAM Compute ASIC Fabrication

Design Document

SDMay26-22

Dr. Duwe & Dr. Wang

Vinicius Malaman Soares

Ali Mannan

Austin Miller

Tyler Kloser

sdmay26-22@iastate.edu

sdmay26-22.sd.ece.iastate.edu

Revised: May 8, 2026

Executive Summary

The exponential growth of Artificial Intelligence (AI) and Machine Learning (ML) has created a critical demand for energy-efficient computing architectures. Traditional Von Neumann architectures struggle with the latency and power consumption associated with moving massive amounts of data between memory and processing units during vector multiplication tasks . Resistive Random Access Memory (ReRAM) offers a promising solution through Compute-In-Memory (CIM), where analog matrix multiplication occurs directly within the memory array. However, the integration of ReRAM into standard CMOS processes, specifically the open-source Skywater 130nm PDK, lacks sufficient characterization data. Without a reliable understanding of device physics, process variation, and programming dynamics in this specific node, designing robust large-scale CIM accelerators remains impractical.

Our team is designing a ReRAM Characterization Vehicle to address this gap. Rather than attempting a full-scale computer immediately, this Application Specific Integrated Circuit (ASIC) is designed as a research platform to quantify the behavior of Skywater 130nm ReRAM cells. The design targets the ChipFoundry May 13th shuttle and utilizes a strictly open-source toolchain (XSchem, Magic, NGSPICE).

The chip architecture features four distinct "Investigation Areas" designed to isolate specific performance variables:

1. Device Physics & Variation: A "Process & Size Variation Array" containing 1T1R (1 Transistor, 1 Resistor) cells of varying pillar sizes (minimum, 2x, 4x) and physical locations. This module will allow for statistical analysis of cycle-to-cycle and device-to-device conductance variation.

2. Scalability & IR Drop: Dedicated "Column Droop" structures (8-cell and 32-cell columns) with fully pinned-out bit lines and word lines to experimentally measure voltage loss across long arrays, validating simulation models for future scaling.

3. Programming Dynamics: Structures designed to support external precision pulsing, enabling the generation of "tuning curves" that map pulse width and voltage to successful SET/RESET states.

4. Component Verification: A set of standalone analog blocks—including a Transimpedance Amplifier (TIA), 1-bit ADC, and 1-bit DAC—alongside a bare 2x2/4x4 crossbar to establish baseline performance metrics for the peripheral circuitry required for CIM operations.

Technical implementation has progressed significantly. The team has successfully installed and verified the open-source toolchain and overcome early model convergence issues. Furthermore, we have achieved reliable simulation of the 1T1R cell performing SET and RESET operations and are currently finalizing the layout for the variation arrays. This project provides the essential empirical foundation required for future high-density ReRAM compute designs at Iowa State University.

Learning Summary

Development Standards & Practices Used

Development Engineering Standards (see Section 2.2)

- IEEE 1481-2019: IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)
- IEEE 1076.4-2000: IEEE Standard VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification
- IEEE 2427-2025: IEEE Approved Draft Standard for Analog Defect Modeling and Coverage

Design Practices

- Adhere to open-source ChipFoundry tool-flow
  - Circuit design: XSchem
  - Simulation: NGSPICE
  - Layout and parasitic extraction: Magic
  - Pre-check: ChipFoundry/Efabless tools
- Git for version control
- All devices included in Skywater 130nm PDK
- Individual pin-out on every completed module
- Baseline characteristics catalogued for every mixed-signal module (e.g., gain, bandwidth, and slew rate of op-amps)

Summary of Requirements

- Characterization vehicle of ReRAM technology
- Bare, individually characterizable crossbars (1x1, 4x1, 8x1, 2x2, 4x4)
- Experimentation with various sizes of ReRAM
- Measure cycle-to-cycle and resilience of 1T1R cells
- Measure effect of other mixed-signal components (TIA, DAC, ADC) on output of ReRAM crossbar

Applicable Courses from Iowa State University Curriculum

- CPRE 2810 – Digital Logic
- CPRE 3810 – Computer Architecture
- EE 3300 – Integrated Electronics
- EE 4650 – Digital VLSI Design
- EE 4350 – Analog VLSI Design

New Skills/Knowledge Acquired That Was Not Taught in Courses

- Resistive memory technology
- Compute in memory architectures
- Open-source VLSI tools (e.g., XSchem, Magic, NGSPICE, and the ChipFoundry tool-flow with the Skywater 130nm process)

Contents

1 Introduction **9**

1.1 Problem Statement . . . 9

1.2 Intended Users . . . 10

2 Requirements, Constraints, And Standards **11**

2.1 Requirements & Constraints . . . 11

2.2 Engineering Standards . . . 12

3 Project Plan **13**

3.1 Project Management/Tracking Procedures . . . 13

3.2 Task Decomposition . . . 13

3.3 Project Proposed Milestones, Metrics, and Evalutation Critera . . . 14

3.4 Project Timeline/Schedule . . . 15

3.5 Risks and Risk Management/Mitigation . . . 15

3.6 Personnel Effort Requirements . . . 17

3.7 Other Resource Requirements . . . 17

4 Design **18**

4.1 Design Context . . . 18

4.1.1 Broader Context . . . 18

4.1.2 Prior Work/Solutions . . . 18

4.1.3 Technical Complexity . . . 19

4.2 Design Exploration . . . 19

4.2.1 Design Decisions . . . 19

4.2.2 Ideation . . . 19

4.2.3 Decision-Making and Trade-Off . . . 20

4.3 Proposed Design . . . 21

4.3.1 Overview . . . 21

4.3.2 Detailed Design and Visual(s) . . . 21

4.3.3 Functionality . . . 26

4.3.4 Areas of Concern and Development . . . 27

4.4 Technology Considerations . . . 27

4.5 Design Analysis . . . 28

4.5.1 Inverter . . . 28
4.5.2 1T1R Cell . . . 30
4.5.3 Operational Amplifier . . . 31
4.5.4 Transmission Gate . . . 34
4.5.5 Analog to Digital Converter . . . 36
4.5.6 AND Gate . . . 36
4.5.7 XOR Gate . . . 37
4.5.8 Full 1-bit Design . . . 37

5 Testing **39**

5.1 Unit Testing . . . 39
5.2 Interface Testing . . . 39
5.2.1 Method 1: I-V Sweeps (Device Physics) . . . 40
5.2.2 Method 2: Pulse Dynamics (Tuning Curves) . . . 40
5.2.3 Method 3: Statistical Endurance Testing . . . 40
5.2.4 Method 4: IR Drop Measurement . . . 40
5.2.5 Method 5: Component Baseline Characterization . . . 40
5.3 Integration Testing . . . 41
5.4 System Testing . . . 41
5.5 Acceptance Testing . . . 41
5.6 User Testing . . . 41
5.7 Precheck Testing . . . 42
5.7.1 Precheck Criteria and Design Requirements . . . 42
5.7.2 Environment Setup . . . 42
5.7.3 Component Verification . . . 45
5.7.4 Klayout Tools . . . 45
5.8 Bring Up Plan . . . 46
5.9 Results . . . 46
5.9.1 Inverter . . . 46
5.9.2 1T1R . . . 47
5.9.3 4x4 Crossbar . . . 51
5.9.4 AND gate . . . 53
5.9.5 XOR gate . . . 54

5.9.6 Amplifier as a Comparator . . . 55
5.9.7 Full 1-bit compute module . . . 56

6 Professional Responsibility **58**

6.1 Areas of Responsibility . . . 58
6.2 Project Specific Professional Responsibility Areas . . . 58
6.3 Virtues . . . 59

7 Closing Material **62**

7.1 Conclusion . . . 62
7.2 References . . . 62

8 Team **64**

8.1 Team Members . . . 64
8.2 Required Skill Sets . . . 64
8.3 Skill Sets Covered . . . 64
8.4 Project Management Style . . . 64
8.5 Initial Project Management Roles . . . 65
8.6 Team Contract . . . 65

List of Figures

1 Projected Gantt chart of project timeline . . . 15
2 Proposed Design High Level Block Diagram . . . 21
3 Schematic drawing of 1T1R Array and analog MUX . . . 22
4 Schematic drawing of IR droop characterization . . . 23
5 Schematic drawing of mixed-signal components . . . 24
6 High-level view of a 2x3 crossbar . . . 25
7 High-level view of a 1T1R schematic . . . 26
8 XSchem schematic of inverter . . . 28
9 Layout view of inverter . . . 29
10 XSchem schematic of 1T1R . . . 30
11 Layout view of 1T1R . . . 30
12 XSchem schematic of 5T operational amplifier . . . 31
13 Layout view of 5T operational amplifier . . . 32
14 XSchem schematic of two-stage operational amplifier . . . 33
15 Layout view of two-stage operational amplifier . . . 33
16 XSchem schematic of transmission gate . . . 34
17 Layout view of transmission gate . . . 35
18 XSchem schematic of the 2-bit ADC . . . 36
19 XSchem schematic of the AND Gate . . . 36
20 XSchem schematic of the XOR Gate . . . 37
21 XSchem schematic of full 1-bit design . . . 38
22 File Setup . . . 42
23 Inverter in Harness Example . . . 43
24 Comment in .spice file . . . 43
25 Documentation Example . . . 44
26 CLI GPIO program . . . 44
27 Log of failed precheck . . . 45
28 Log of passing precheck . . . 45
29 Log of failed XOR test . . . 45
30 Command to start Klayout . . . 45
31 Klayout with specific layers . . . 46

32 XSchem schematic of inverter . . . 46
33 Simulation results of inverter . . . 47
34 XSchem schematic of 1T1R . . . 47
35 ReRAM characteristics after SET operation . . . 48
36 ReRAM characteristics after RESET operation . . . 49
37 Simulation results of 1T1R . . . 49
38 SET of 1T1R with WL toggle . . . 50
39 RESET of 1T1R with WL toggle . . . 51
40 XSchem schematic of 4x4 crossbar . . . 52
41 Simulation results of 4x4 crossbar . . . 53
42 Simulation results of a 00 input . . . 53
43 Simulation results of a 01 input . . . 53
44 Simulation results of a 10 input . . . 54
45 Simulation results of a 11 input . . . 54
46 Simulation results of a 00 input . . . 54
47 Simulation results of a 01 input . . . 54
48 Simulation results of a 10 input . . . 55
49 Simulation results of a 11 input . . . 55
50 Comparator testing results . . . 56
51 XSchem schematic of full 1-bit design . . . 56
52 Sample result for input HIGH and SET ReRAM, output HIGH . . . 57

1 Introduction

1.1 Problem Statement

With the increased demand for AI, many are trying to find ways to make the computations needed more efficient. AI tasks utilize a great amount of vector algebra, particularly vector multiplication. Resistive Ram (ReRam) is a relatively recent component for placing in an integrated circuit (IC). that can store different information based on the resistance of a cell. A ReRam crossbar is a specific architecture that allows for computations within itself, namely vector multiplication. The benefit of doing these computations inside the memory cell allows for better efficiency in terms of both power and time. By doing these calculations in the analog domain, results can be obtained faster and do not rely on data being read from memory, manipulated in an arithmetic unit, and results written back to memory.

When running inference on a Machine Learning model, part of the computation of the final output of each convolution layer is computed by matrix dot multiplication. Multiplications over a large number of layers can be time and energy consuming. Each time a model computes a singular output it may need hundreds of millions of Multiply and Accumulate operations for that to happen. Besides the time it takes to compute each of these operations, another time and energy consuming operation is the data transfer from memory to where the computation happens. As the number of necessary MAC operations grows, so does the latency due to this transfer.

Conventional computer architecture handles these MAC operations using the Von Neumann cycle, where an instruction is fetched, decoded, and then executed. This execution is then stored in memory.

Our solution is to do the MAC operations using memory components (ReRAM), hence named compute-in-memory. This eliminates the need for data transfer between a processing module and a memory module. Ultimately working to optimize speed and reduce unnecessary power consumption. Additionally, there may be some extra performance gains coming from the fact that the compute is done using the innate physical laws of electricity (namely Kirchoff's laws) and not through the digital processing done in a CPU.

The main issues our design runs into are reliability, since our computations are done in the analog domain, our architecture will need to make significant concessions to ensure a high noise margin, so the compute does not come out with the wrong answer, and the result of the compute is deterministic. We will have to design our architecture with noise margins in mind, and this likely means sacrificing some potential performance gains.

The goal of the project after building a working model is to test the noise-tolerancy, and report on it's potential application as a real substitute for conventional computing in the context of machine learning.

1.2 Intended Users

Iowa State Professors/Researches - The main client and intended user for this project is our client Dr. Wang, a professor and researcher at Iowa State University in the Electrical and Computer Engineering Department. It will be use to assist in the characterization of the ReRAM module.

Machine Learning Developers - Machine learning algorithms using large language models are taking over the commercial business to be able to help their customers learn more about their business by asking specific questions. This user needs to be able to answer their customers' questions while not having a designated person answer everyone so having an AI that is trained for their business would make it more efficient for the company. Using ReRAM technology would help businesses run the AI model in a more efficient and less costly manner in terms of power required and the number of executable instructions machine learning requires.

Iowa State Students - Iowa State students interested in Semiconductor design/fabrication and students interested in Hardware design for ML/AI applications are eager to learn about new technologies being developed and tested in the field. Our project provides just that. It is an opportunity for upcoming students in future years to test out our physical chip as well as our design.

2 Requirements, Constraints, And Standards

2.1 Requirements & Constraints

Functional requirement: Organized repository of hardware and software components

One of the more considerable deliverables and requirements for this project is an open repository with all design files. Since the use of ReRAM technology for in-memory computing is still in the research stage, it is important to leave a clean and organized repository for the next teams to come. By leveraging the repository we leave, future teams researching the same topic can make more rapid progress and hopefully with fewer mistakes.

Functional requirement: Use of open-source tools (Constraint)

One of the main goals behind this project is to keep making progress using what was left for us from previous teams, and to leave our work for future teams. To ensure that our project can be used by anyone, one of the constraints is to use open-source software in our design. Using tools that are available for everyone ensures that our project can be used and run by others, even against unforeseen events.

Functional Requirement: Device Physics & Variation Characterization

The design must enable the quantification of ReRAM resistance and switching behavior with respect to physical size and die location. To achieve this, the system must include a "Process & Size Variation Array" consisting of 16 individual 1T1R structures divided into four groups: minimum-sized ReRAM, medium-sized (2x area), large-sized (4x area), and a physically distant minimum-sized group to measure location-based variation. Per client requirements, the transistor size must remain constant while only the ReRAM pillar size varies.

Functional Requirement: Statistical Analysis Capability

The design must support statistical data collection to characterize the variability of the ReRAM technology. This includes measuring cycle-to-cycle variation (e.g., conductance changes within a single device over $> 10^3$ cycles) and device-to-device variation (performance spread across identical devices in different physical locations)

Functional Requirement: Array Scalability & IR Drop Measurement

To characterize the scaling limits of the technology, the design must allow for the direct measurement of IR drop (voltage droop) across bit/source lines. The layout must include "Column Droop Test Structures" (e.g., 8-cell and 32-cell columns) with bit lines and word lines pinned out for precise external voltage sensing under load.

Functional Requirement: Programming Dynamics & Endurance Testing

The system must support the characterization of programming pulse parameters (voltage and duration) and operational lifetime. The design must provide pin-out access to allow external precision pulse generators to sweep pulse widths and read cell states, creating device "tuning curves" and measuring cycle-to-failure rates.

Functional Requirement: System Component Verification

The design must demonstrate the functionality of the compute-in-memory building blocks. This requires independent "Standalone Analog Blocks" (TIA, ADC, DAC) and a "Bare Crossbar Array" (2x2 or 4x4) with direct external connections to establish baseline performance before full system integration.

Resource requirements: Open-source tools and the Skywater 130nm Process must be used, along with all design files passing to precheck, in order to be manufactured by ChipFoundry.

Deadline requirement: ChipFoundry May 13th shuttle.

Constraints: Design area and I/O pins are predicted not to be a problem, but there is a possibility that our project may face area constraints or I/O pin availability issues since the design is to be manufactured along with several other senior design/ChipForge projects. Due to the high number of terminals required for the characterization arrays (48+ terminals), extensive analog multiplexing or shared control lines will be required to fit within the pad frame. Additionally, power, interconnect, design rules, and thermal constraints are set to not exceed the Skywater 130nm process specifications

2.2 Engineering Standards

- **Standard 1: IEEE 1481-2019 IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)**

  Standard that pertains to how IC designers log and analyze performance parameters of their designs. Particularly by characterizing the performance with respect to timing and power. Our project consists almost entirely of designing analog ICs, therefore characterizing our circuits according to this standard fits our needs.

- **Standard 2: IEEE 1076.4-2000 IEEE Standard VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification**

  This standard defines methods that promote highly accurate and efficient simulations for ASIC design. This fits our project since simulation is a crucial part of the design process of this project.

- **Standard 3: IEEE 2427-2025 IEEE Approved Draft Standard for Analog Defect Modeling and Coverage**

  This standard pertains to how IC designers test their circuits and quantitatively discusses a testing strategy for detecting defects, to ensure a standardized metric of defects among analog ICs. Our project consists of a significant number of analog ICs, and the goal is to manufacture in the Skywater 130nm process. This means that the final product will need to be characterized, which includes the defects.

3 Project Plan

3.1 Project Management/Tracking Procedures

The project management style our team chose was waterfall. Each component in our ReRAM design requires each component to be built linearly so we can have a steady progression towards the final tapeout for the ReRAM crossbar. Each component requires many steps so planning for the requirements and use of the individual component is essential for the design.

For tracking progress for our design, we will be using Microsoft Teams to rely on any information about upcoming milestones and deliverables to ensure everyone is up to date about the progress going forward for the project and any issues that arise when designing, testing, or simulating.

3.2 Task Decomposition

The following is a breakdown of the steps to complete the design.

Task 1: Installing and understanding the Skywater PDK toolflow

- Install toolflow
- Understand how the different programs interact with each other
- Create a basic inverter and run the design through precheck to have a clear goal of how to design each component

Task 2: Design of Core 1T1R & Variation Modules (Module A)

- Design and simulate the baseline 1T1R cell.
- Layout generation for the "Process & Size Variation Array" (Min, Medium, Large pillars).
- Critical Sub-task: Verify simulation convergence for the ReRAM model, which has been a documented hurdle.

Task 3: Design of Signal Integrity Structures (Module B)

- Create the "Column Droop" test structures (8-cell and 32-cell columns).
- Implement full pin-outs for word lines and shared bit lines to enable direct IR drop measurement.

Task 4: Standalone Analog Block Verification (Module C)

- TIA: Design and layout of the Transimpedance Amplifier with tunable gain for sensing diverse resistance states.
- ADC/DAC: Validation of 1-bit and multi-bit converters to serve as baseline references for quantization error.

Task 5: Pad Frame Integration & I/O Management

- Constraint Management: Map the 48+ required test signals to the limited available pads on the Caravel harness.
- Design and validate analog multiplexers (MUX) to share I/O pads where necessary.

Task 6: Final Tapeout Assembly

- Integrate Modules A, B, C, and D into the final user area wrapper.
- Run final LVS (Layout vs. Schematic) and DRC (Design Rule Check) on the combined system.
- Submit for Pre-check and Tapeout

3.3 Project Proposed Milestones, Metrics, and Evalutation Critera

With each design component, there is a process that components must go through to ensure proper functionality

Schematic

- Design of the component

Testbench

- Test the schematic for normal operation and edge cases with the intent to understand faults within the design

Layout

- Run the design through Design Rule Checker (DRC) and Layout vs Schematic (LVS) to ensure proper layout

Post-Layout Characterization

- Extract the parasitic parameters of the layout to ensure proper physical characteristics
- Check timing, power, path delays, setup and hold times
- Run layout through precheck to ensure proper functionality for fabrication For each component there are also certain metrics that have been formulated to ensure a working design

Milestone 1: Reliable Simulation

- Metric: Successful simulation of FORM, SET, and RESET cycles in NGSPICE without convergence errors.

Milestone 2: Module A (Variation Array) Readiness

- Metric: Layout must pass DRC/LVS with parasitics extracted.
- Criterion: All 16 cells must be independently addressable (via pads or Mux) to allow for the collection of device-to-device statistical data.

Milestone 3: Signal Integrity Validation

- Metric: The "Column Droop" structure must allow for the resolution of < 10mV voltage drops across the bit line to quantify IR loss accurately.

Milestone 4: Analog Baseline Performance

- Metric: TIA must demonstrate > 10dB gain and sufficient bandwidth (> 10MHz) to distinguish between High Resistance State (HRS) and Low Resistance State (LRS) during read operations.

Milestone 5: Pre-Check Passage

- Metric: Zero DRC violations and clean LVS matches for the integrated pad frame.
- Criterion: Design must be successfully accepted by the ChipFoundry submission portal.

3.4 Project Timeline/Schedule

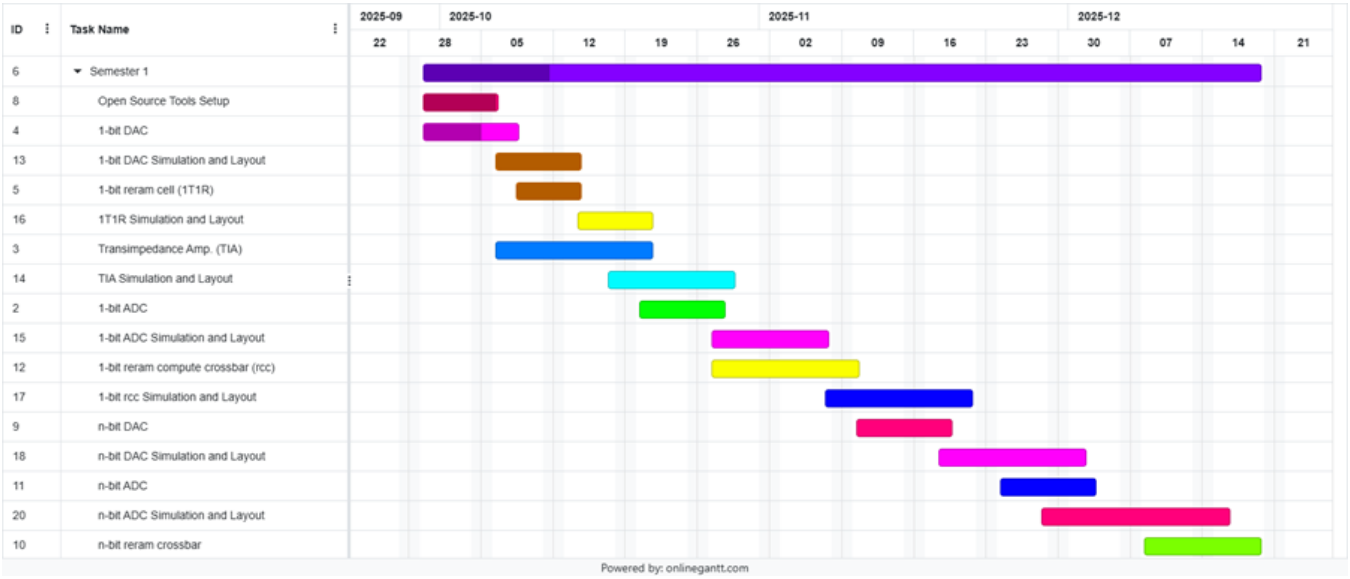


Figure 1: Projected Gantt chart of project timeline

3.5 Risks and Risk Management/Mitigation

Following are the risks that are expected to be encountered, and the associated mitigation plan.

Risk: Simulation Convergence & Model Accuracy (Probability: High)

• *Description*: Throughout the design phase, the team encountered significant issues with the ReRAM SPICE model failing to simulate or converging on incorrect states.

• *Mitigation*: We have established a standardized VM environment to ensure tool version consistency. Additionally, we are including "Standalone Analog Blocks" (Module C) that do not rely on the ReRAM model, ensuring that at least part of the chip can be characterized even if the ReRAM cells behave unexpectedly.

Risk: I/O Pad Limitation (Probability: High)

• *Description*: The characterization plan requires accessing over 48 individual terminals (Source Lines, Bit Lines, Word Lines) for the variation arrays. The Caravel harness has a fixed number of GPIO/Analog pads.

• *Mitigation*: We are prioritizing "Primary Goals" (Section 2.1) for dedicated pads. For secondary signals, we are designing simple analog multiplexers to route multiple internal test points to a single external pad.

Risk: Process Variation & Device Failure (Probability: Medium)

• Description: ReRAM technology is susceptible to manufacturing variation, where devices may be "stuck" in a specific state or vary wildly in resistance.

• *Mitigation*: We are implementing the "Process & Size Variation Array" (Module A) with redundancy (4 cells per group) . If one cell fails, others in the group can still provide statistical data. We are also including physically distant groups to account for spatial variation on the die.

3.6 Personnel Effort Requirements

Task Breakdown

Task	Description	Hours
Tool Setup	Setting up the open-source tools with a Linux environment	16
1-bit DAC	Schematic and layout of a 1-bit Digital-to-Analog Converter	24
Operational Amplifier	Schematic and layout for an Operational amplifier to be used in multiple parts	24
1-bit ADC	Design and test of a 1-bit Analog-to-Digital converter	8
1-bit ReRAM cell	Design and test of a 1-bit ReRAM cell	24
1-bit ReRAM compute module	Design and test of a 1-bit Compute module ReRAM	24
n-bit ReRAM crossbar	Design and test of an n-bit ReRAM crossbar	24
n-bit ADC	Design and test of an n-bit Analog to Digital converter	32
Test and Characterization	Test and characterization of the final design, before being submitted	24

3.7 Other Resource Requirements

Our resource requirements are minimal, due to our usage of mainly open-source tools and the client-provided funding and structure for the tape-out. The work of previous senior design teams will be heavily referenced and built-upon, as well as communication with the engineers that worked on it.

4 Design

4.1 Design Context

4.1.1 Broader Context

Area	Description	Examples
Public health, safety, and welfare	The ReRAM can present the benefit of reducing the energy consumption it takes to perform matrix vector multiplication.	Decreasing the power consumed by massive data centers can improve the electrical grid reliability of communities.
Global, cultural, and social	This project uses only open-source tools, and all the work done will be open-sourced.	With the project being open to everyone, we hope to inspire others to work on a project related to ReRAM.
Environmental	One of the possible benefits of the ReRAM module is the reduced energy consumption for matrix-vector multiplication—the computation behind all AI models.	With the potential cut in power consumption, the datacenters powering AI will have their impact on the Power Grid reduced.
Economic	With ReRAM being in its early stages of research and development, the improvement made in the area could result in an industry being created around the technology.	Any characterizations made by our client in the future can help further propel the investment by companies in the technology, creating more market growth and potential jobs.

4.1.2 Prior Work/Solutions

ISAAC: A Convolutional Neural Network Accelerator with In-Situ Analog Arithmetic in Crossbars [1]

This research paper uses a ReRAM crossbar setup, similar to what we are trying to achieve. They had a similar setup with the DAC and crossbar, but they use a Sample and Hold before the ADC. Overall, it provides a solid baseline for what has been accomplished in the field and what may be improved.

SDDec24-13

This senior design team concluded in December of 2024. Their setup consisted of an eight-by-eight array of ReRAM cells using a 1T1R setup. Their documentation is available on the senior design website and provides insights into what worked and where expectations fell short. This documentation helps reduce redundant tasks. In the end, our advisor informed us that their fabricated chip never returned from fabrication.

SDMay25-19

This senior design team concluded in May of 2025. Their setup focused on multiple ReRAM designs for characterization, similar to our goals. The final design included four ReRAM crossbars — two from previous senior design teams and two original designs of their own. Their chip is still in fabrication, but if delivered before our final design is complete, we can use it for testing and characterizing designs of our own.

4.1.3 Technical Complexity

Resistive Random Access Memory (ReRAM)

As ReRAM is a new and emerging technology, it requires extensive research, testing, and documentation of its characteristics.

Design of OpAmp, TIA, ADC, and DAC

In the complete ReRAM crossbar setup, multiple peripheral analog circuits are required, including OpAmps, Transimpedance Amplifiers, and data converters. These peripherals are complex and time-consuming to design. Each must be tailored to specific applications, requiring thoughtful design iteration.

Use of Open-Source Tools

This project relies entirely on open-source software. The combination of new tools and limited developer support presented a steep learning curve.

Characterization Decisions

Important engineering decisions must be made in alignment with the client's expectations. Our final design must consider the client's needs and adapt accordingly.

4.2 Design Exploration

4.2.1 Design Decisions

Characterization Options

For our design, we selected characterization goals that align with the client's research interests.

Analog-to-Digital Converter Design

There are many ADC architectures, and we must choose the one that best fits our requirements.

Operational Amplifier Design

There are numerous design approaches for OpAmps, and we must select the technique appropriate for our specifications.

4.2.2 Ideation

For the peripheral circuitry, especially the analog-to-digital converter, there are multiple design paths available. Many variables must be evaluated before choosing a design. We investigated several ADC architectures and identified five of the most promising options:

- Flash ADC
- Sample & Hold

- Pipelined ADC
- Successive Approximation Register (SAR) ADC
- Delta-Sigma ADC

4.2.3 Decision-Making and Trade-Off

When deciding on which characterizations to move forward with, the decision came down to prioritizing the ones that will enable the client to perform critical characterizations and tests.

- Primary
  - Single ReRAM
    - Single ReRAM will help the client to characterize the behavior of a single cell to be used as a base line
  - Full 1-bit Design
    - Full 1-bit design informs the client of ReRAM behavior with auxiliary analog components in a 1-bit enivronment with a functional DAC, operational amplifier, and ADC
  - IR drop
    - Columns allow for measuring the voltage drop down Bit lines or word lines and is important because this drop can affect results of the computation when scaled up and placed into the compute crossbar
    - A big problem with ReRAM technology is accounting for the IR drop when calculating matrix vector multiplication because the slightest drop will produce different values so analyzing why the drop occurs and by how much will help produce a more precise crossbar calculation.
- Secondary
  - Bare crossbar
    - Testing the bare crossbar in simulation is one of the goals that the client would be happy to see, but it is not a must for us.
- Tertiary

  Full crossbar with DAC, ADC, and TIA

  Currently these are not necessarily required from our client to perform but would create an easier to read and understand intersection from the chip to any microprocessor we choose to incorporate with

4.3 Proposed Design

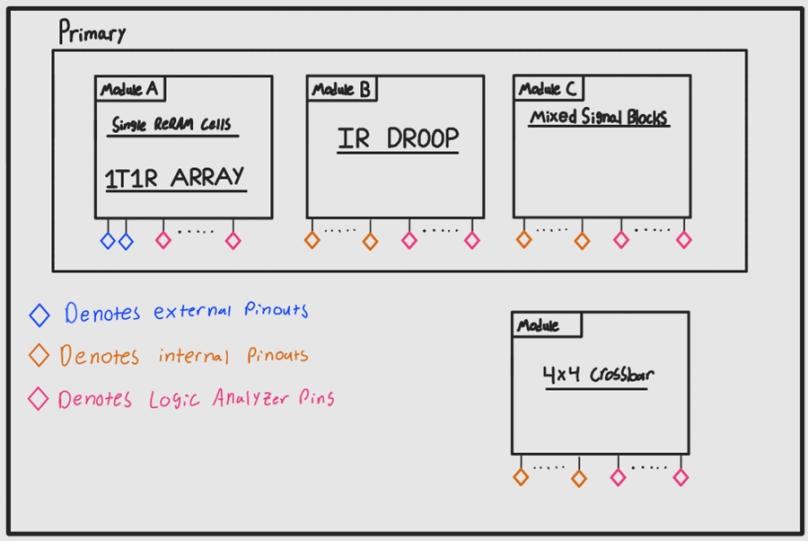


Figure 2: Proposed Design High Level Block Diagram

4.3.1 Overview

Our design has evolved from a single compute module to a collection of distinct test structures sharing a common die, serving as a *ReRAM Characterization Vehicle*. While the long-term goal of the technology is in-memory computation, the immediate priority is to quantify the behavior of the ReRAM cells provided by the Skywater 130nm process, to inform the viability of using the cells in a compute in-memory architecture.

The design includes four specific modules: a Process & Size Variation Array, Column Droop Test Structures, Standalone Analog Blocks, and a Bare Crossbar Array. These modules share a common pad frame but operate independently to allow for isolated characterization of device physics, programming dynamics, and signal integrity.

4.3.2 Detailed Design and Visual(s)

Below are listed several modules that are intended for characterization.

Module A: Process & Size Variation Array

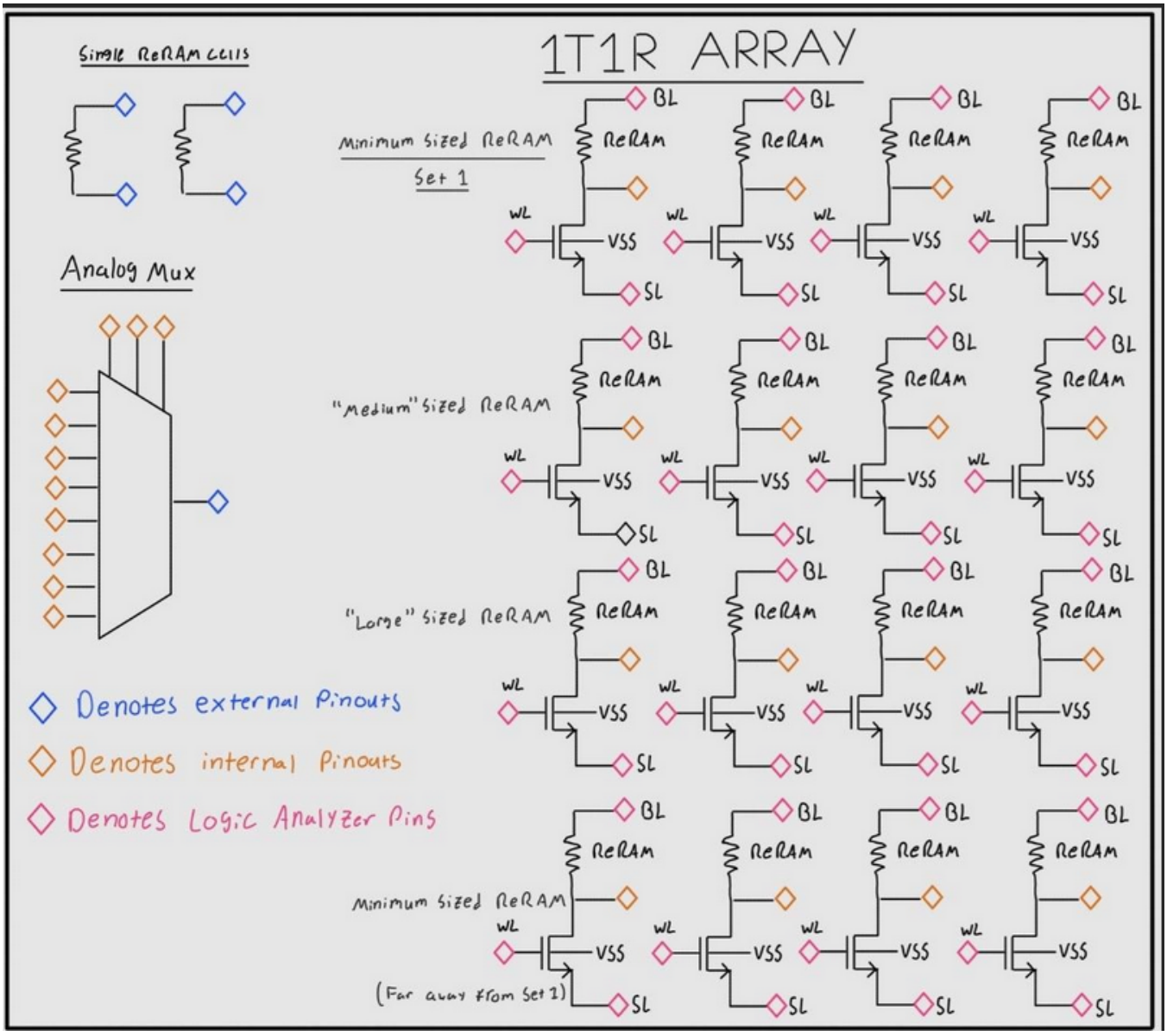


Figure 3: Schematic drawing of 1T1R Array and analog MUX

- A 16-cell array of 1T1R (1 Transistor, 1 Resistor) structures organized into four groups of four cells.
- Group 1: 4 cells with a minimum-sized ReRAM layout.
- Group 2: 4 cells with a medium-sized (2x area) ReRAM layout.
- Group 3: 4 cells with a large-sized (4x area) ReRAM layout.
- Group 4: 4 cells with a minimum-sized ReRAM layout placed physically distant from Group 1 to measure spatial variation.

Design Note: Per client feedback, we are varying the ReRAM pillar size while keeping the access transistor size constant to isolate geometric effects. We are also exploring the inclusion of standalone ReRAM cells (without transistors) for baseline testing.

Module B: Column Droop & Scalability Structure

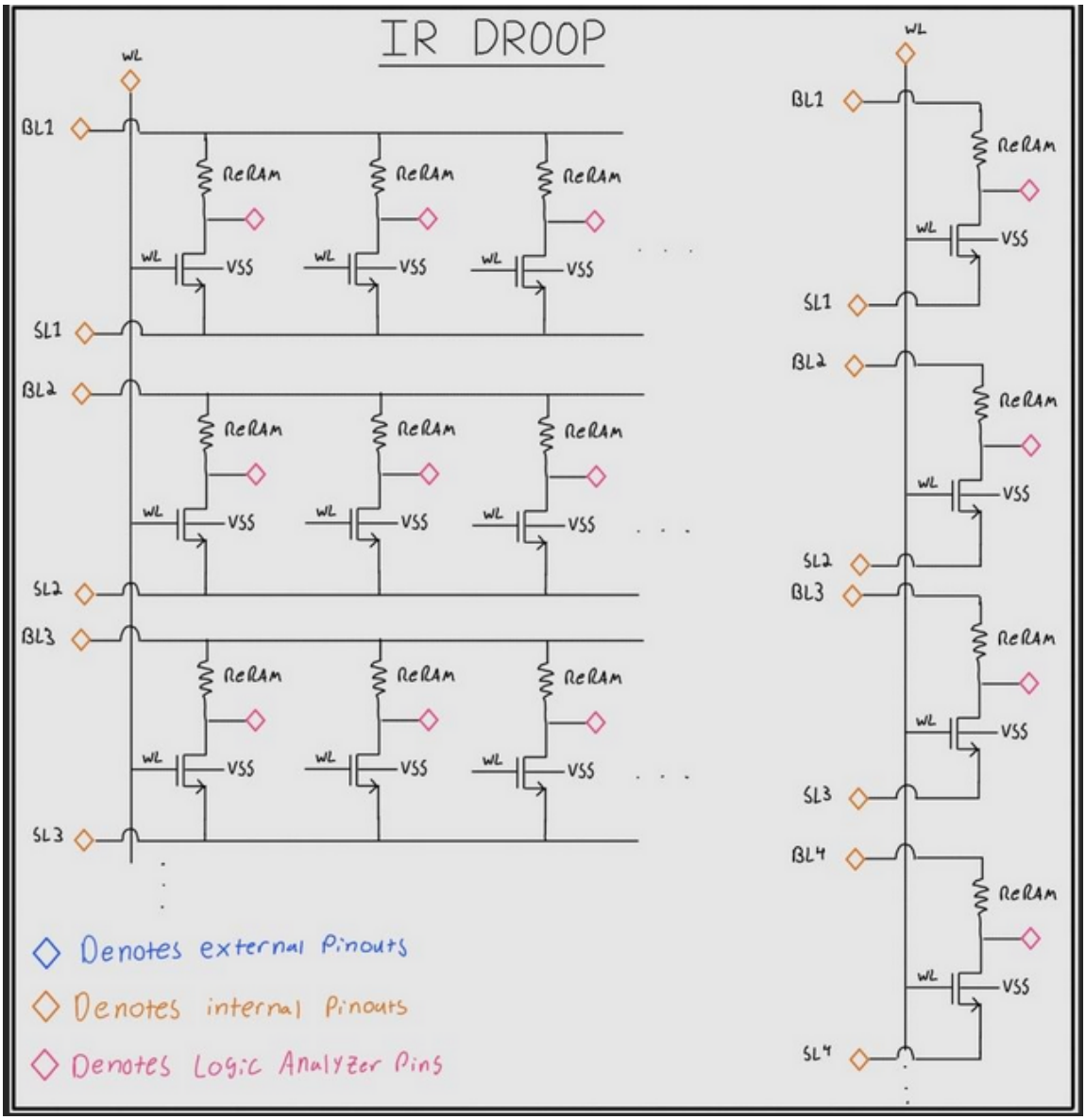


Figure 4: Schematic drawing of IR droop characterization

- Two dedicated columns of 1T1R cells: one short column (8 cells) and one long column (32 cells).
- For each column, the shared bit line has pads at both ends to allow current forcing and voltage sensing.
- Every word line is pinned out to a dedicated pad to ensure individual cell selection.

Module C: Standalone Analog Block

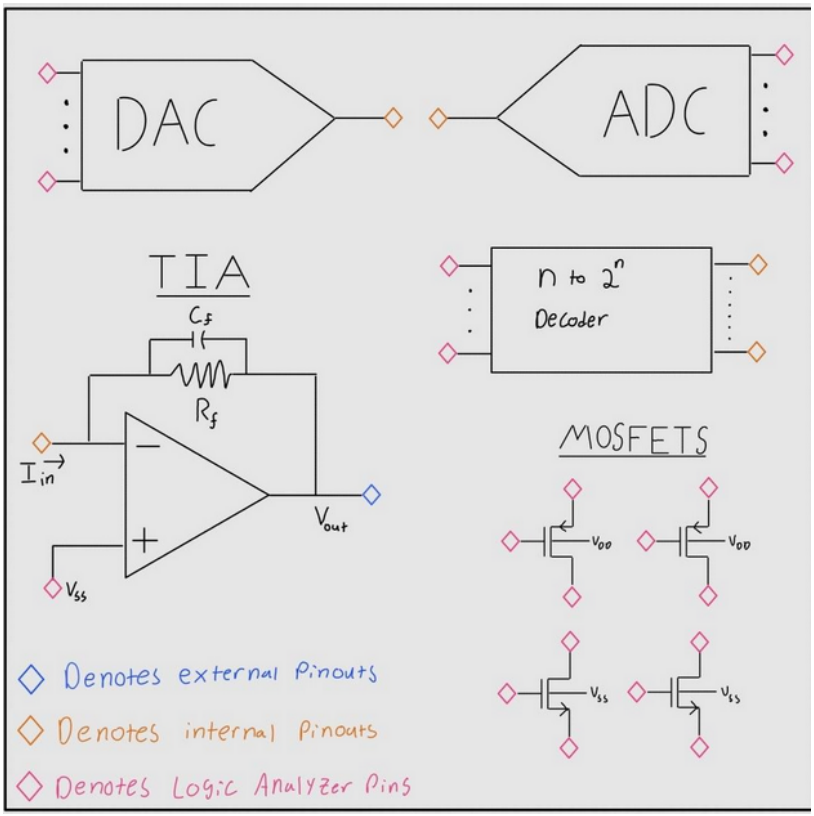


Figure 5: Schematic drawing of mixed-signal components

- Isolated peripheral circuits included to characterize their behavior independent of the ReRAM arrays.
- TIA: Transimpedance Amplifier designed for $> 10\,\text{dB}$ gain and $> 10\,\text{MHz}$ bandwidth.
- ADC/DAC: 1-bit and multi-bit converters for characterizing quantization error, offset, and noise.

Module D: Bare Crossbar Array

- A 2x2 and/or 4x4 crossbar array of 1T1R cells without on-chip peripherals. All word lines, bit lines, and source lines are internally pinned, allowing for digital control of forming/setting/resetting cells, along with reading them from the logic analyzer pins.

The tertiary goal is to complete a full crossbar design. It would be the complete crossbar implementation with the DAC, TIA and ADC. The full design can be found in figure 4.1. The ReRAM cells are denoted by the resistor, and the impedance of each ReRAM cell can be configured to match an expected value beforehand. When looking in a setting of the applications for AI, the ReRAM cells' impedance would relate to a weight value of a neuron, and the DAC would produce the input value. The value at the TIA would be the sum of the inputs multiplied by their

respective weight values. This is also shown in the next figure. The value at the TIA is the sum of input 1 times weight 11 and input 2 times weight 12.

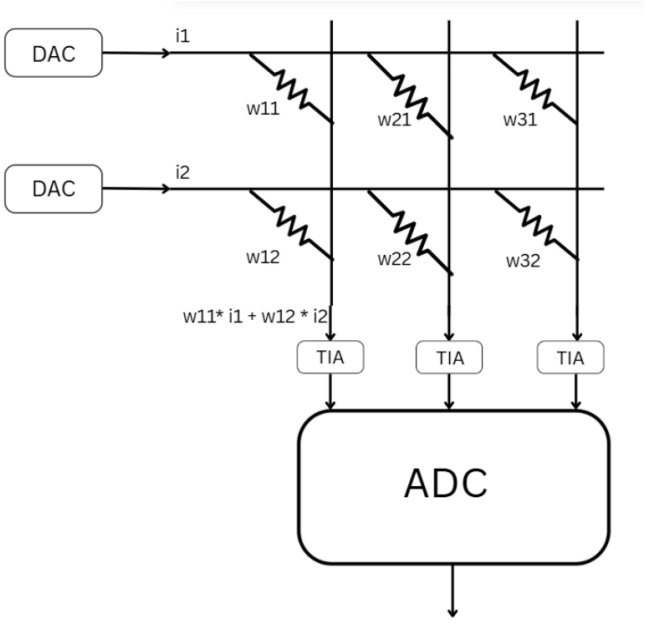


Figure 6: High-level view of a 2x3 crossbar

Each ReRAM cell will be broken down into one resistor and one transistor, this setup is referred to as 1T1R. In this setup we have the resistor in series with the Drain of a MOSFET and the Bit Line. The Bit Line will be our value coming from our DAC and will be connected to the ReRAM. The Word Line is connected to the Gate of the MOSFET and will decide if the cell is being used or not. The Select Line is connected to the Source of the MOSFET and will be the line going towards the TIA.

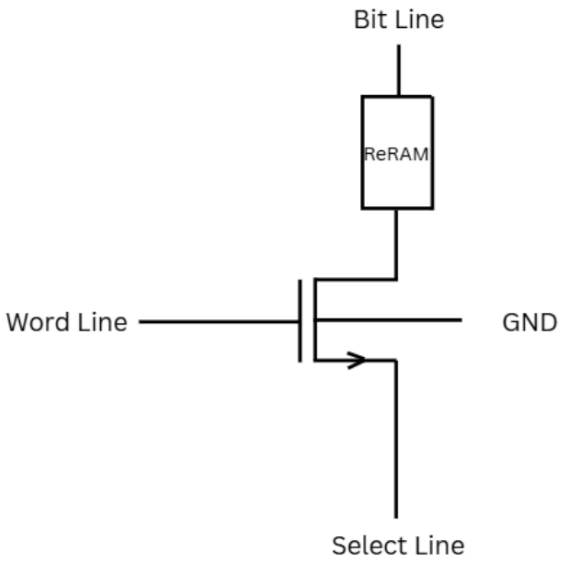


Figure 7: High-level view of a 1T1R schematic

4.3.3 Functionality

The intention of our ReRAM Crossbar design is to be an instructional vehicle for Iowa State University to further develop an understanding of how this emerging technology can be used efficiently. The main goal is to test the limitations of the basic modules of a crossbar to find out possible read and write speeds, physical limitations like sensitivity to noise and outside factors like functionality in different temperatures, and the best possible use when it comes to matrix vector multiplication, and compare the results to a standard MAC design within an Arithmetic Logic Unit. With the use of an FPGA, these tests can provide valuable feedback. Outside the use of the university, our design will help future designers understand how a ReRAM Crossbar operates and provide a solid foundation for how one may go about designing IC's with the Skywater 130nm ReRAM technology. Unlike a standard memory chip, this design prioritizes observability over density. It allows researchers to:

1. Generate "Tuning Curves": By sweeping external voltages, we can determine the optimal pulse width and voltage required to FORM, SET, and RESET the cells.

2. Quantify IR Drop: By measuring the voltage difference across the "Column Droop" structures, we can experimentally validate simulations of signal loss in larger arrays.

3. Statistical Analysis: The array structure allows for gathering statistical distributions of High-Resistance States (HRS) and Low-Resistance States (LRS) across multiple devices and cycles.

The intention with our ReRAM Crossbar design is to be an instructional vehicle for Iowa State University to further develop an understanding about how this emerging technology can be used efficiently. The main goal is to

test the limitations of the Crossbar to find out possible read/write speeds, physical limitations like sensitivity to noise and outside factors like functionality in different temperatures, and the best possible use for when it comes to matrix vector multiplication and compare the results to a standard MAC design within an Arithmetic Logic Unit. With the use of an FPGA, these tests can provide valuable feedback.

Outside the use of the university, our design will help future designers understand how a ReRAM Crossbar operates and provide a solid foundation for the proper best case uses for this new technology.

4.3.4 Areas of Concern and Development

The main concern about this project is the possibility of not producing any output. The concern stems from the fact that there are a lot of moving parts in a final complete design of a ReRAM crossbar that could present errors. At the same time, our client's main goal is to characterize different parts of the design and different parameters. As a plan to address both the concern of not having an output and the need of the client, we plan on adding different measurement points along multiple essential parts of the design. That allows us to still produce multiple outputs that our client can use to measure different aspects of the design they are interested in.

4.4 Technology Considerations

Our design is to be built using the SkyWater 130 nm process and will be fabricated using ChipFoundry's May (ReRAM) shuttle. The ChipFoundry precheck process (the final step before fabrication) is based on the Efabless chip design toolflow. This technology path is non-negotiable, as our client has entered into an agreement with ChipFoundry and has already committed to the May 2026 tapeout.

The complete design and simulation environment is open-source. This includes XSchem for schematic entry, Magic VLSI for layout and parasitic extraction, NGSPICE for SPICE-level simulation, and the ChipFoundry/Efabless analog toolflow for final manufacturing preparation. While XSchem and Magic could theoretically be replaced with commercial tools such as Cadence Virtuoso, no funding exists for such licenses and these tools do not integrate well with the Efabless toolchain.

Summary of Tools

- **XSchem** – schematic implementation and SPICE netlist generation
- **NGSPICE** – SPICE simulation and waveform analysis
- **Magic VLSI** – layout implementation and parasitic extraction
- **ChipFoundry tool-flow** – hardening and manufacturability checks for final tapeout

4.5 Design Analysis

Installation and running of the tools was an expected challenge that has been overcome. The following are analog and mixed-signal components that have been designed and tested.

4.5.1 Inverter

The design of the inverter was set to be minimally sized, as this component was seen to behave as expected with minimal effects seen from parasitic resistances and capacitances. The deisng is futher discussed in Section 5.8.1. A schematic of the inverter is given by the figure below.

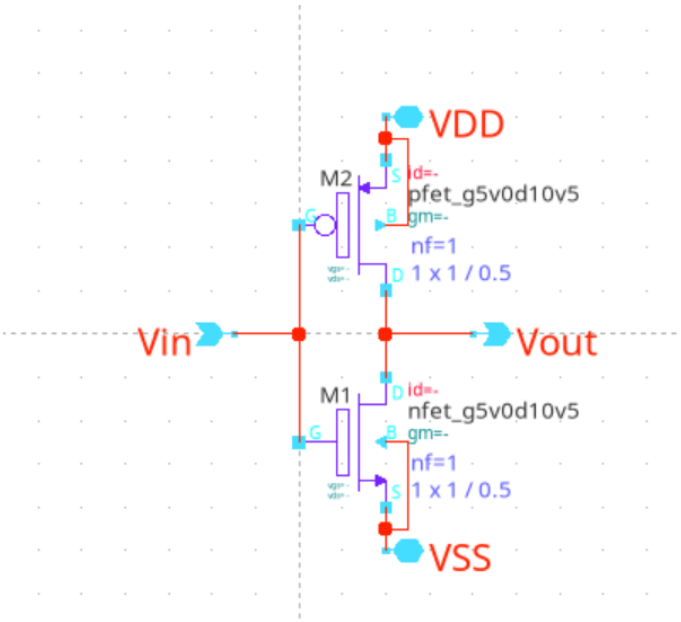


Figure 8: XSchem schematic of inverter

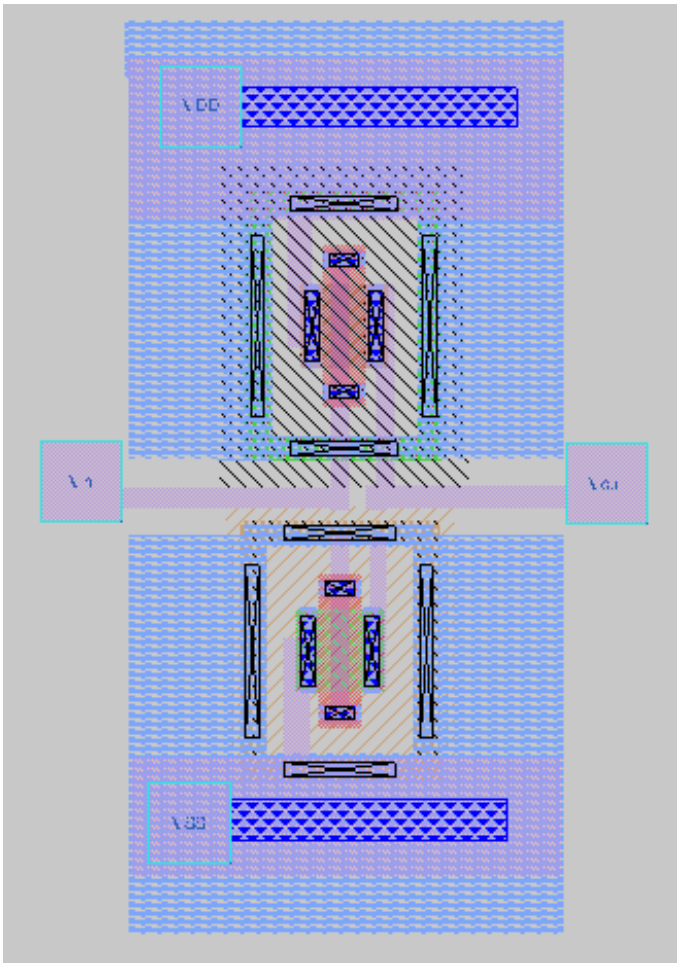


Figure 9: Layout view of inverter

4.5.2 1T1R Cell

The design of the 1T1R features a minimally sized NMOS transistor that acts as an electrically controlled switch (controlled by WL: word line), this switch determines if current flows through the ReRAM module. BL (bit line) and SL (source line) are manipulated in order to perform SET/RESET/READ operations on the ReRAM cell.

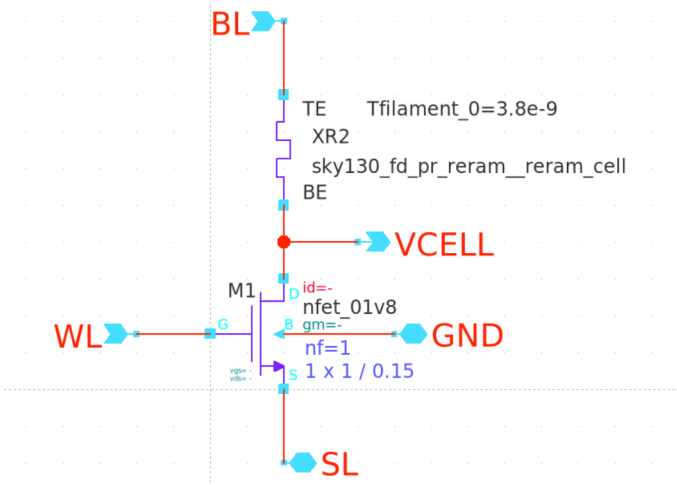


Figure 10: XSchem schematic of 1T1R

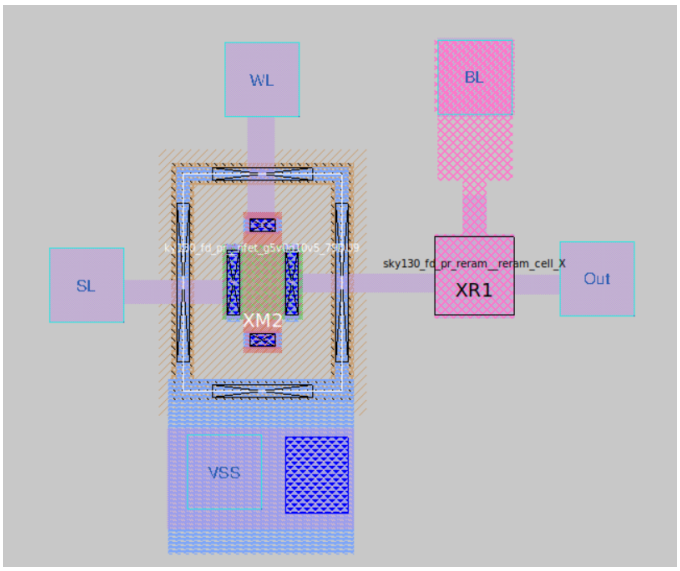


Figure 11: Layout view of 1T1R

4.5.3 Operational Amplifier

The design of the operational amplifier was completed to provide a DC gain of 100dB to behave acceptably as a comparator in the ADC. The operational amplifier was also designed for a gain-bandwidth product in the GHz range. Two different amplifier architectures were implemented, two-stage and 5-transistor. The design for the two-stage amplifier is largely in credit to the prior work of previous senior design team sddec24-11.

See testing section for details on amplifier implementations.

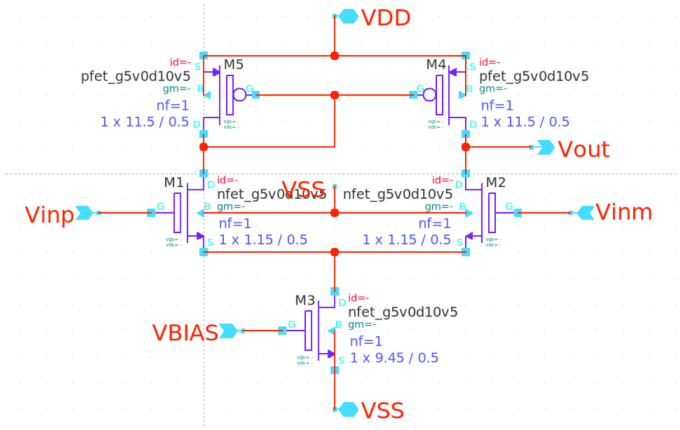


Figure 12: XSchem schematic of 5T operational amplifier

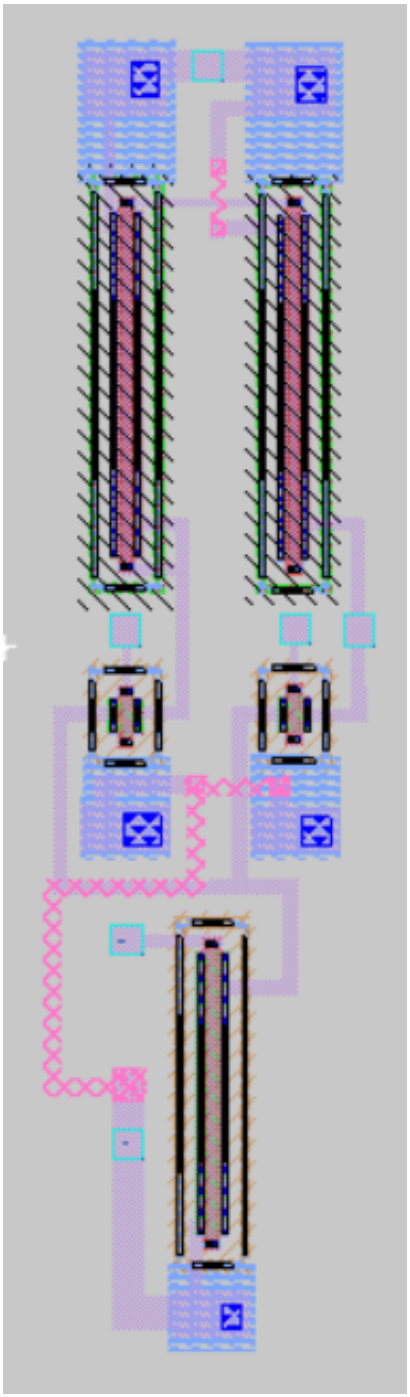


Figure 13: Layout view of 5T operational amplifier

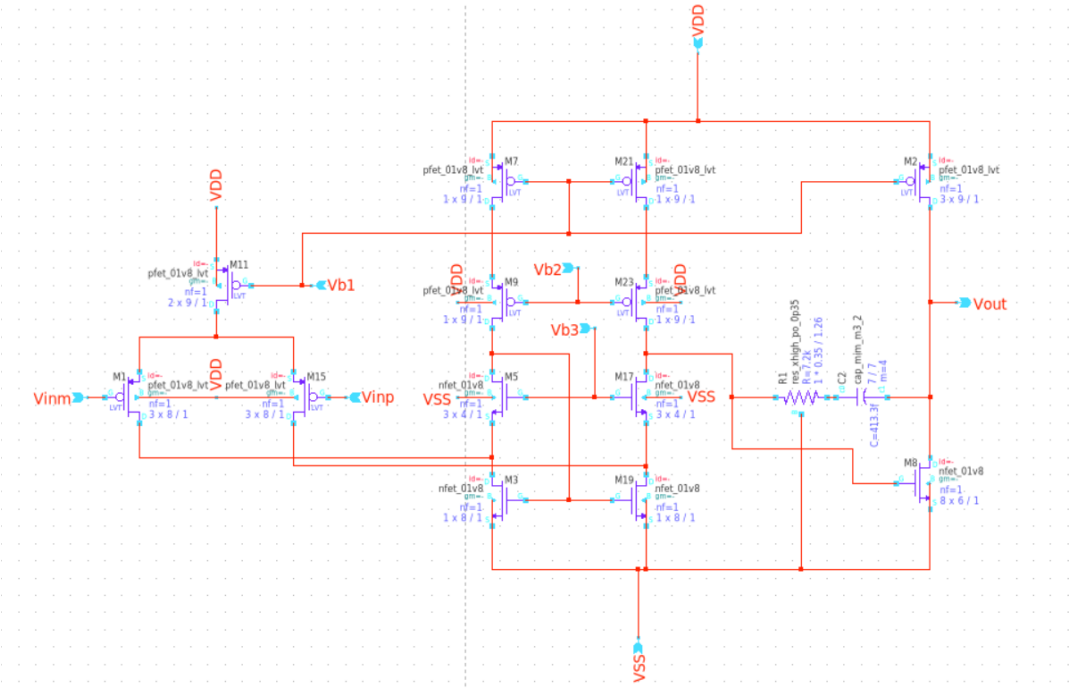


Figure 14: XSchem schematic of two-stage operational amplifier

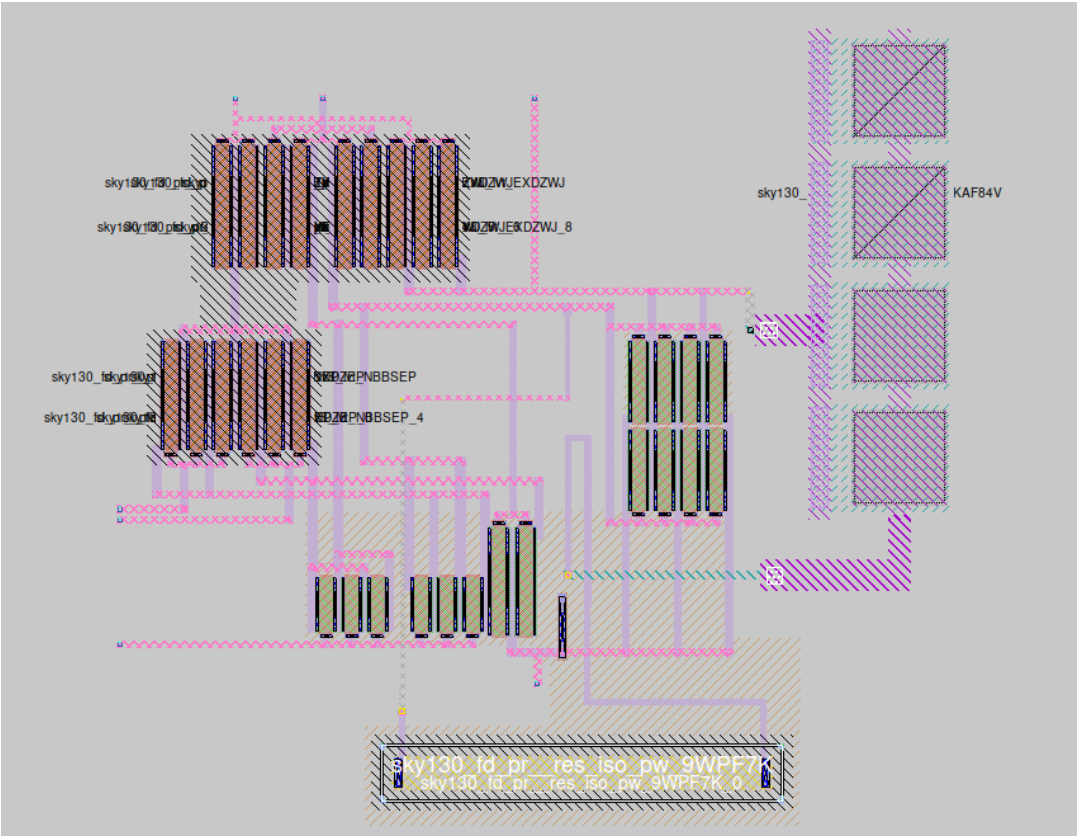


Figure 15: Layout view of two-stage operational amplifier

4.5.4 Transmission Gate

The transmission gate was sized to achieve equal rise and fall times.

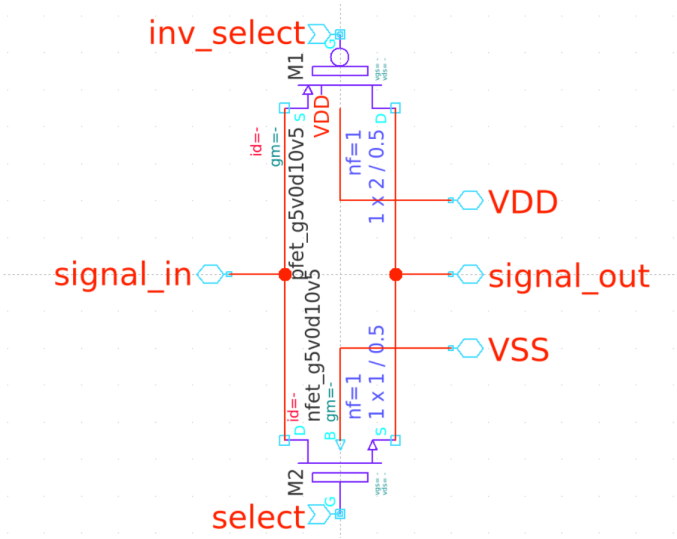


Figure 16: XSchem schematic of transmission gate

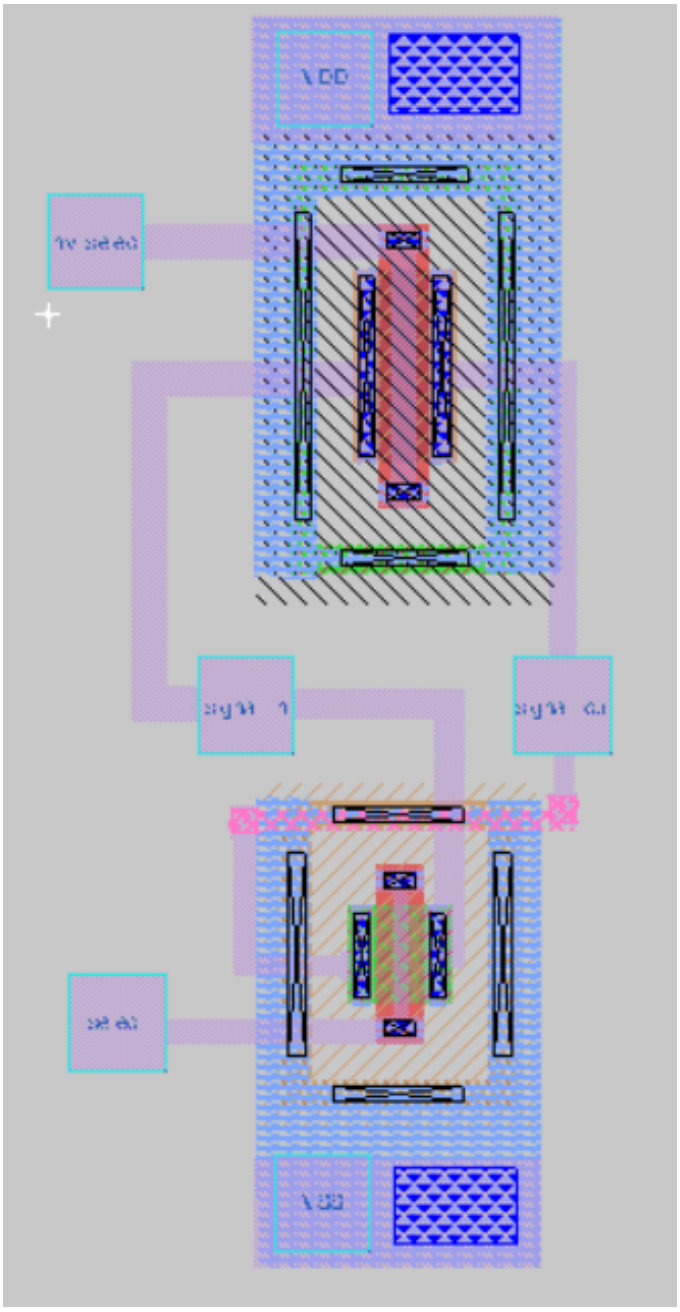


Figure 17: Layout view of transmission gate

4.5.5 Analog to Digital Converter

To assist with the data conversion of crossbar sets larger than 1-bit, a 2-bit flash ADC was designed. The design uses 3 Operational Amplifiers as comparators, and later fed into a priority encoder for a 2-bit output.

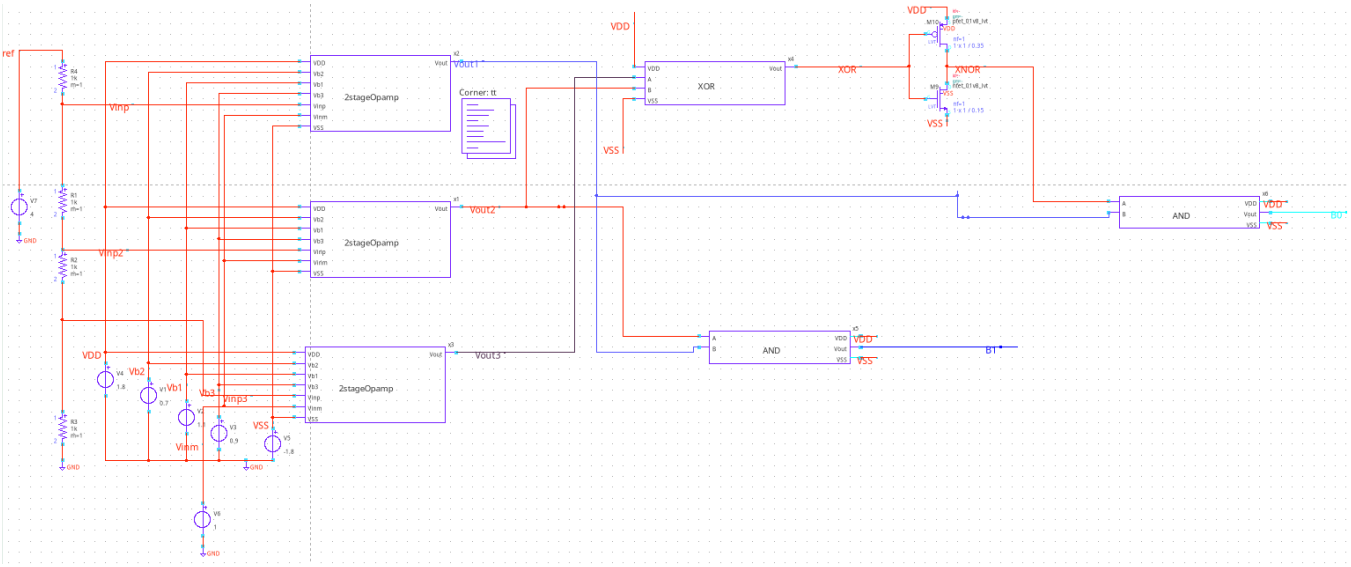


Figure 18: XSchem schematic of the 2-bit ADC

4.5.6 AND Gate

The AND gate was designed to take two inputs and have a high output only if both inputs are high.

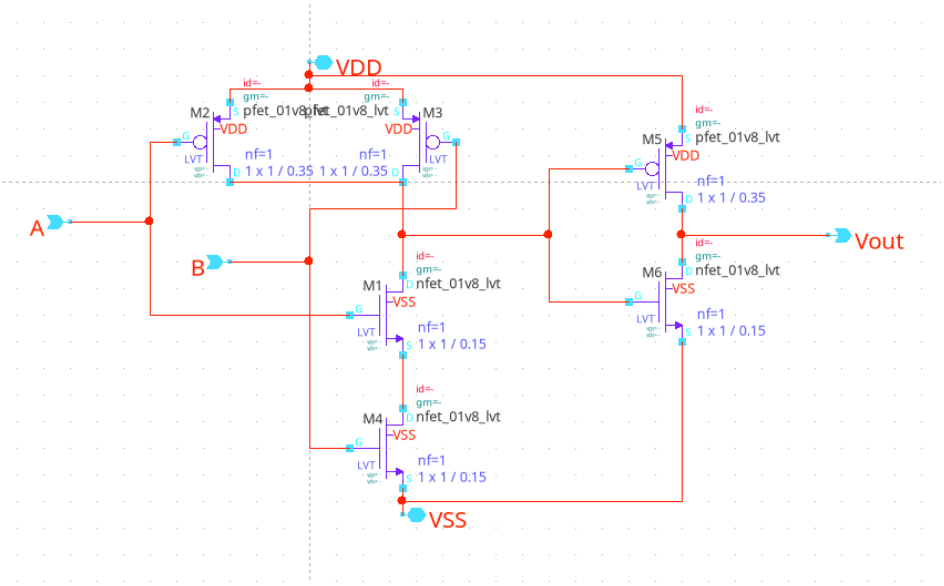


Figure 19: XSchem schematic of the AND Gate

4.5.7 XOR Gate

The XOR gate was designed to accept two inputs and produces an output that is high when one of the inputs is high and the other is low, and a low output otherwise.

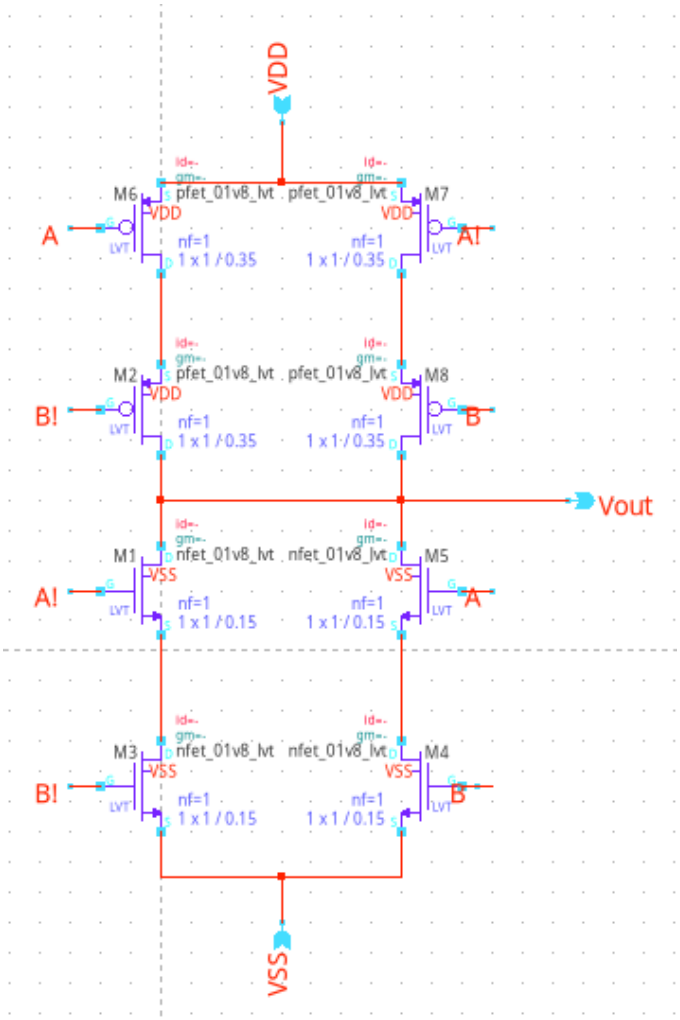


Figure 20: XSchem schematic of the XOR Gate

4.5.8 Full 1-bit Design

The full 1-bit design was completed, using an inverter for the DAC, transmission gates as switches for isolation, an operational amplifier used in open-loop as a comparator, to an analog out pin.

It was seen from testing that:

- Resistance of ReRAM on SET = 9216Ω
- Resistance of ReRAM on RESET = 2.5MΩ

The following equation sizes the resistor RX feeding into the bit line BL:

$$V_{BL} = V_{DD}(\frac{R_{ReRAM}}{R_X + R_{ReRAM}})$$

$$R_X = 150k\Omega$$

A Vref to be compared using the comparator was chosen using the following relation:

$$V_{ref} = \frac{V_{BL_{RESET}} + V_{BL_{SET}}}{2}$$

$$V_{ref} = 0.9V$$

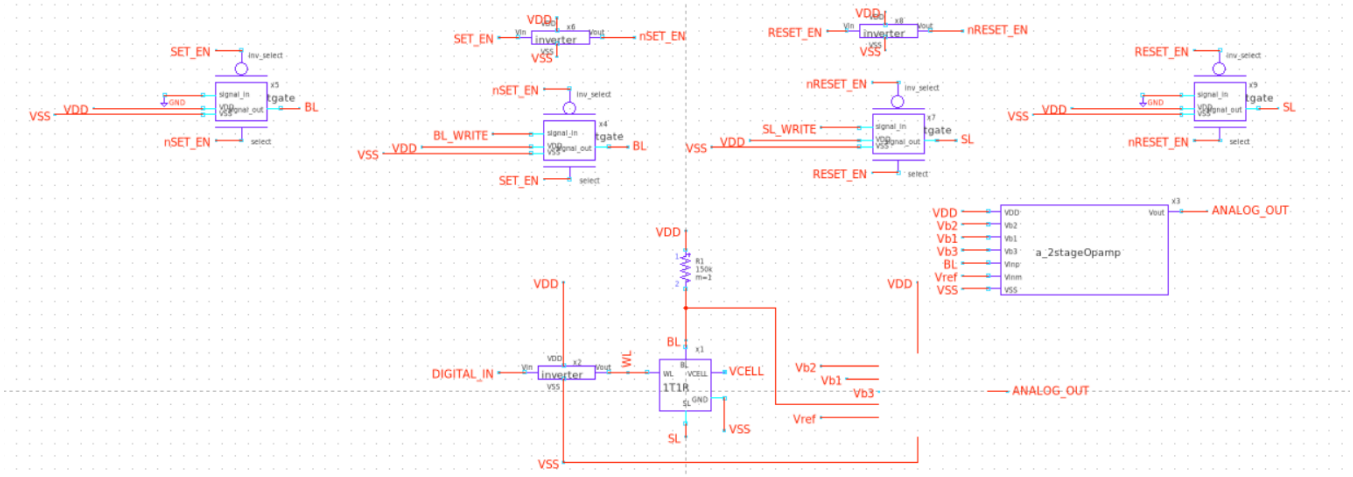


Figure 21: XSchem schematic of full 1-bit design

5 Testing

A big part of the deliverable asked by the client, is the ability to characterize different parts of the design and different designs as a whole. To achieve the best possible scenario, all the units involved in the design will be tested. We will be testing the different peripheral circuits (DAC, ADC, etc.) and our core circuits (1T1R, 2x2 crossbar, etc.). To perform such tests we will be using the Open-Source tools XSchem and Ngspice. XSchem is the tool used to design the schematics for our designs, so where the circuits will be designed and built. Ngspice will allow us to perform spice simulations, on those designs.

5.1 Unit Testing

The eventual high-level compute module can be split into the following categories:

- DAC (Digital-to-Analog Converter)
- ReRAM Crossbar
- TIA (Transimpedance Amplifier)
- ADC (Analog-to-Digital Converter)

The client requests that each individual part of the design can be characterized for research purposes, most importantly the ReRAM crossbar. During the design process, each component is created using XSchem, and a layout with parasitic extraction is completed through Magic VLSI. The circuits are simulated and waveforms are viewed through NGSPICE and Gaw.

A big part of the deliverable asked by the client, is the ability to characterize different parts of the design and different designs as a whole. To achieve the best possible scenario, all the units involved in the design will be tested. We will be testing the different peripheral circuits (DAC, ADC, etc.) and our core circuits (1T1R, 2x2 crossbar, etc.). To perform such tests we will be using the Open-Source tools XSchem and NGSPICE. XSchem is the tool used to design the schematics for our designs, so where the circuits will be designed and built. NGSPICE will allow us to perform spice simulations, on those designs.

5.2 Interface Testing

The design is split into specific investigation areas, each requiring distinct interface testing methods to characterize the technology.

5.2.1 Method 1: I-V Sweeps (Device Physics)

Using the "Process & Size Variation Array", external test equipment will perform precise Current-Voltage (I-V) sweeps on the pinned-out 1T1R cells. This interface testing will gather statistical data on resistance distributions (RLRS and RHRS), enabling direct comparison between the different size and location groups.

5.2.2 Method 2: Pulse Dynamics (Tuning Curves)

To characterize programming dynamics, an external precision pulse generator will be connected to the pads of the array's cells. The interface test involves sweeping a wide range of pulse widths and voltages while reading the resulting cell state externally. This will generate detailed "tuning curves" required to optimize the programming algorithms for future ReRAM designs.

5.2.3 Method 3: Statistical Endurance Testing

Per client feedback, interface testing must capture statistical variability.

- **Cycle-to-Cycle:** External equipment will apply millions of repeated SET/RESET cycles to a single device (e.g., 10^3 cycles) to measure the variation in conductance over time.
- **Device-to-Device:** The same endurance tests will be run across the physically distant groups in the array to quantify manufacturing variation across the die.

5.2.4 Method 4: IR Drop Measurement

For the "Column Droop" structures, the interface testing involves selecting a specific cell by activating its word line, forcing a known current through one end of the bit line, and sensing the resulting voltage at the other end. This provides a direct, accurate measurement of the voltage droop under specific load conditions.

5.2.5 Method 5: Component Baseline Characterization

The Standalone Analog Blocks (TIA, ADC, DAC) and Bare Crossbar Array have all critical I/O pinned out for isolated characterization. Interface testing will focus on establishing baseline performance metrics—such as TIA gain/bandwidth and ADC offset—before these components are integrated into a full compute system.

Once fabricated, the design is implemented using an on-board RISC-V processor. The fabricated design can also be simulated through the ChipFoundry/Efabless toolflow.

5.3 Integration Testing

The design must critically be able to be characterized, as expressly stated by the client. This means that individual components (such as the ReRAM crossbar) can have their outputs individually observable through different input stimuli.

Firstly, the high-level design must behave as expected, this is obtained by the previously outlined testing methods using XSchem, Magic VLSI, NGSPICE, and Gaw. These tests ensure the individual modules of the design are integrated correctly.

Secondly, the ChipFoundry/Efabless tool-flow must be passed and hooked up to the Caravel harness, and clear pre-check. This step ensures the design gets fabricated correctly and that the design and fabrication are integrated correctly.

5.4 System Testing

System testing steps for high-level components:

1. Create schematics in XSchem.
2. Create testbench in XSchem, simulate using NGSPICE netlist, and view waveforms using Gaw.
3. Import netlist to Magic VLSI, complete layout routing, and pass DRC/LVS.
4. Extract parasitics (capacitance and resistance) from Magic VLSI layout.
5. Simulate design with extracted parasitics and view waveforms using Gaw.

Integration tests are run with the ChipFoundry/Efabless toolflow. integration and after implementation into the overall design. XSchem and NGSPICE are used consistently across all components.

5.5 Acceptance Testing

Two main checks define design acceptability:

1. Simulation results and schematics are reviewed with the client and advisor during weekly meetings.
2. The final design must pass the Efabless precheck and tapeout check prior to the May 2026 tapeout.

5.6 User Testing

Manufacturing a physical prototype is not viable due to cost and tapeout constraints. The primary users are researchers who will utilize the final chip as a research vehicle to characterize ReRAM behavior in the real world. Since chips cannot be manufactured until the planned tapeout, broader user testing is not possible.

5.7 Precheck Testing

To ensure proper submissions for fabrication, ChipFoundry has created its own testing tool flow. This is the final check on all components designed and tested to verify the following criteria.

5.7.1 Precheck Criteria and Design Requirements

The following tests are the criteria precheck verifies:
License, Documentation, Default, Makefile, Top Cell Check, Consistency, GPIO-Defines, XOR, Magic DRC, Klayout FEOL, Klayout Offgrid, Klayout Metal Minimum Clear Area Density, Klayout Pin Label Purposes Overlapping Drawing, Klayout ZeroArea, Spike Check, Illegal Cellname Check, OEB, and LVS.

5.7.2 Environment Setup

There is an analog harness which can be downloaded from their public GitHub, Once in the folder you can terminal to the path and run the following commands "pip install chipfoundry-cli" to install the current CLI tools to set up pin assignments for the harness and "cf setup" to run the script to fully setup all additional tools like Klayout

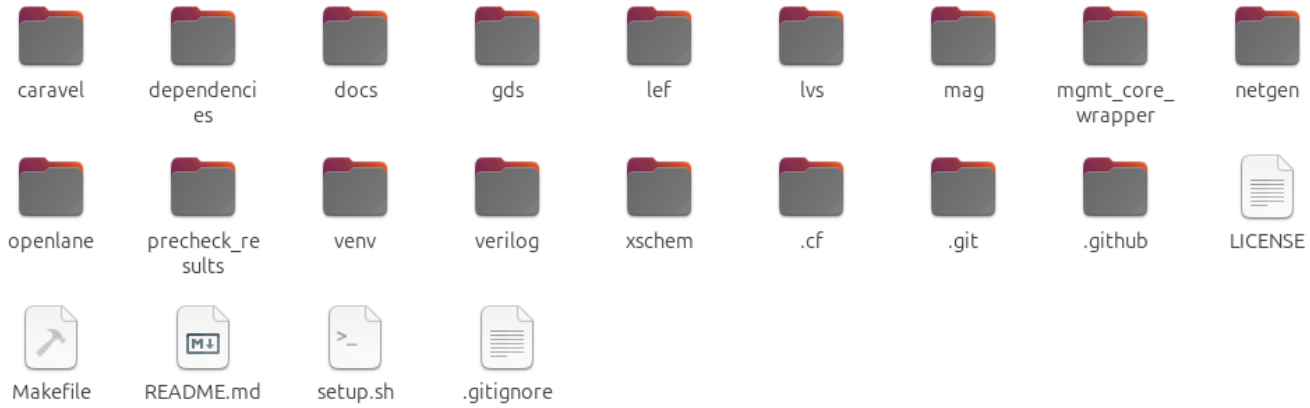


Figure 22: File Setup

For an Analog Project, the main folders a user will interact with are mag, xschem, gds, netgen, and precheck results. Once precheck is complete, all Magic and XSchem project files need to be sorted into their respective folders. Next, any design that needs to be tested must be added to the caravel_user _analog _wrapper _empty and connected to the desired harness pins in Magic.

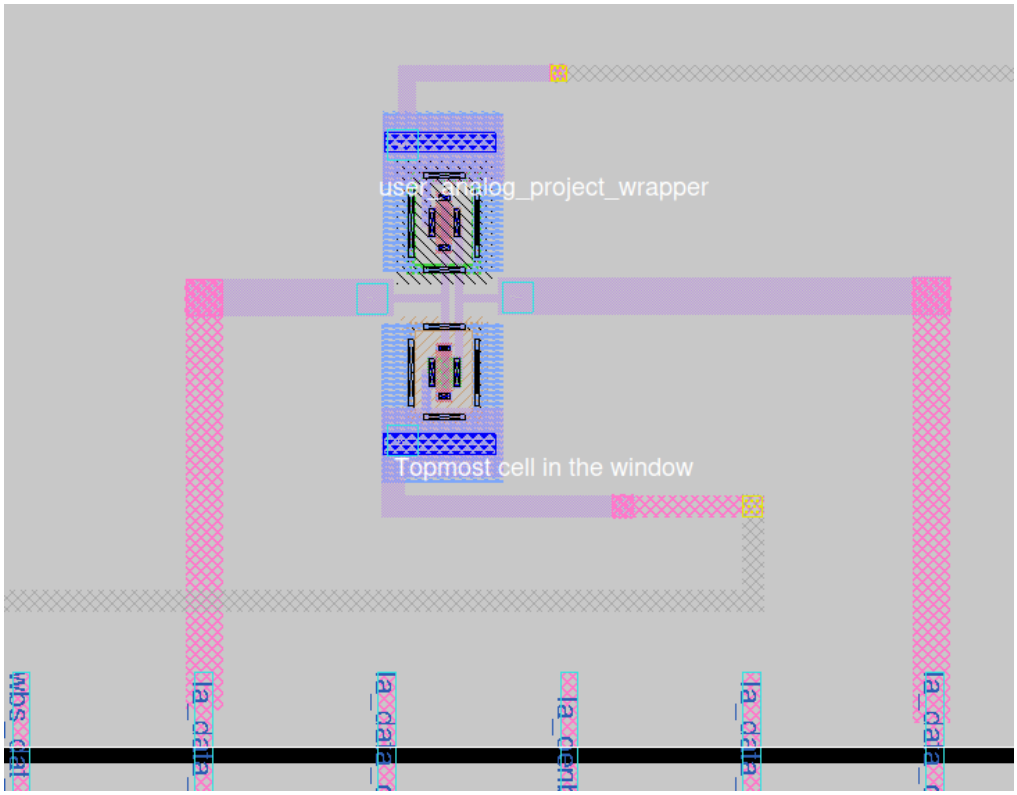


Figure 23: Inverter in Harness Example

Then the spice and gds files for the harness needs to be generated and can be accomplished by using the following commands in the Magic terminal, "extract all", "ext2spice lvs", "ext2spice", "select top cell", "expand, and "gds write ../gds/user_analog_project_wrapper.gds". With the generated spice file in the Mag folder, you can move it to the netgen and xschem folders so precheck can read it.

NOTICE: Currently comments within spice files cause precheck to crash so they need to be removed. For example, this section would need to be removed.

```
*.PININFO vdda2:B vssa2:B vccd1:B vccd2:B vssd1:B vssd2:B wb_clk_i:I wb_rst_i:I wbs_stb_i:I wbs_cyc_i:I wbs_we_i:I
*+ wbs_sel_i[3:0]:I wbs_dat_i[31:0]:I wbs_adr_i[31:0]:I wbs_ack_o:O wbs_dat_o[31:0]:O la_data_in[127:0]:I la_data_out[127:0]:O
io_in[26:0]:I
*+ io_in_3v3[26:0]:I user_clock2:I io_out[26:0]:O io_oeb[26:0]:O gpio_analog[17:0]:B gpio_noesd[17:0]:B io_analog[10:0]:B
io_clamp_high[2:0]:B
*+ io_clamp_low[2:0]:B user_irq[2:0]:O la_oenb[127:0]:I vdda1:B vssa1:B
```

Figure 24: Comment in .spice file

After that step, Documentation must be completed for the component being tested and submitted within the README.md file.

```
# Caravel User Project Analog

## Overview
This project contains a simple inverter integrated into the Caravel analog harness.
It is being used to learn and test the ChipFoundry precheck flow.

## Design
The main top-level cell is `user_analog_project_wrapper`.
The design includes an inverter used as a small analog test structure for checking layout, DRC, and LVS behavior.

## Purpose
The goal of this project is to:
- understand how precheck works
- test wrapper integration
- debug LVS and DRC issues
- verify consistency between layout and netlist

## Files
- `gds/` - GDS layout
- `mag/` - Magic files
- `verilog/` - Verilog sources
- `lvs/` - LVS setup
- `xschem/` - schematic files

## Pins
```

Figure 25: Documentation Example

Then pins must be assigned using the CLI tool, you can start the software using "cf gpio-config". The pins must be setup with input, output, bidirectional, or analog.

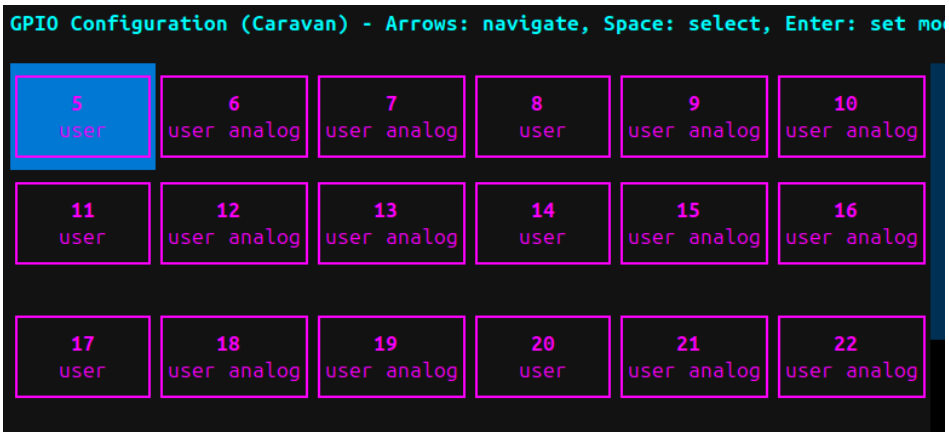


Figure 26: CLI GPIO program

Once that is completed, precheck can be started, first a python virtual environment must be setup, the following commands can be used to accomplish that, "python3 -m venv venv" and "source venv/bin/activate". Now run "cf precheck" to start precheck. The first run can take some time, depending on component design and complexity, but after a report will be generated.

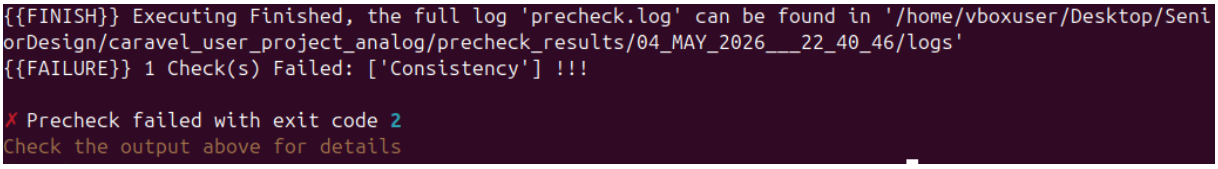


Figure 27: Log of failed precheck

The generated files within precheck results are sorted by each test in outputs which can be used to understand why a specific test failed.

5.7.3 Component Verification

Every component we designed ran through prechecks and troubleshooting until it passed every test.

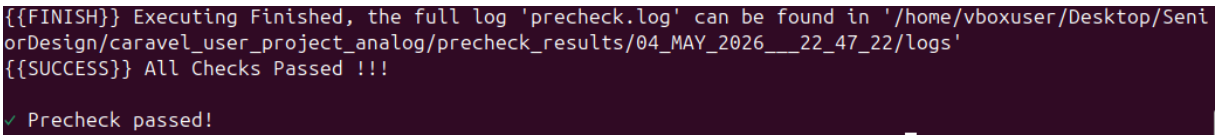


Figure 28: Log of passing precheck

5.7.4 Klayout Tools

Precheck uses Klayout applications to help understand the exact problem that caused a check to fail and where it is within the harness. In this example, I will address an XOR test failure.

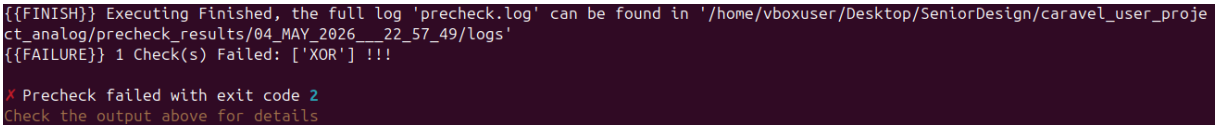


Figure 29: Log of failed XOR test

Klayout can be opened with the following command from the corresponding precheck_results outputs.

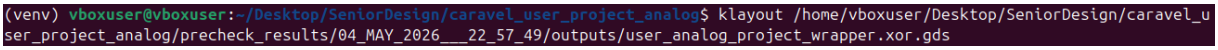


Figure 30: Command to start Klayout

This command will open the Klayout program, which will display the specific coordinates of the problematic area and the layer on which the problem occurs.

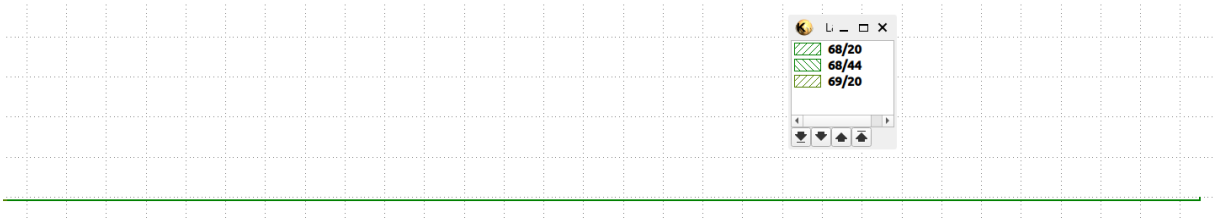


Figure 31: Klayout with specific layers

The following green area can then be traced by location within the mag file for the harness.

5.8 Bring Up Plan

After the crossbar has been fabricated, the built-in Microcontroller will run Verilog tests to verify each category of requirements, creating a seamless testbench that can be used to understand the physical properties of each design. The logic analyzer pins will also be used to create different testing voltages, so the crossbar is not limited to on-board power.

5.9 Results

5.9.1 Inverter

We have been able to simulate two different components of our design, an Inverter(that can serve as a 1-bit DAC) and the 1T1R design. The Inverter was used as shown in the schematic below.

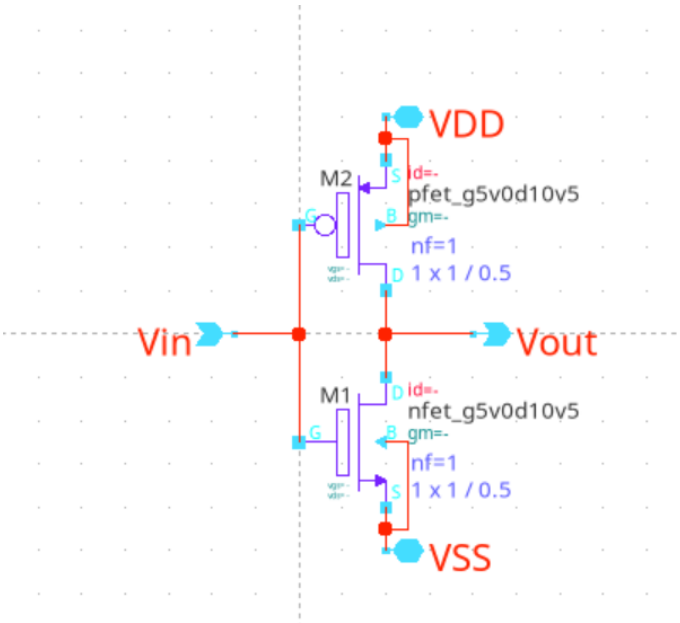


Figure 32: XSchem schematic of inverter

The results of simulating the Inverter are shown below, red represents the input (Vin) and Blue represents the output (Vout). As we can see the result of Vout is LOW when Vin is HIGH and Vout is HIGH when Vin is LOW. The following figure shows the results of simulating the inverter after creating a layout and extracting parasitics of the layout shown in the Design section.

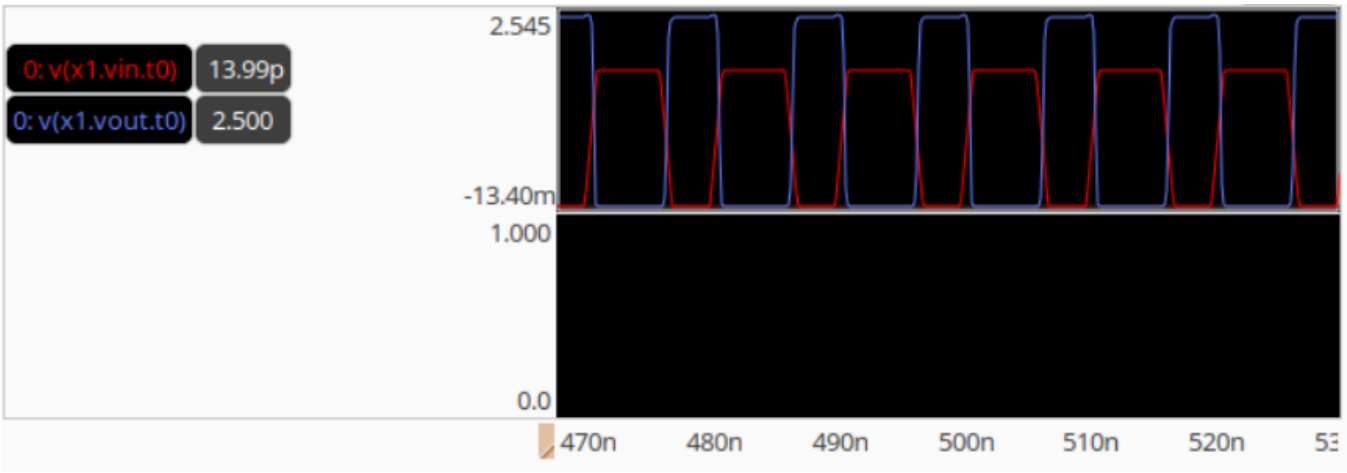


Figure 33: Simulation results of inverter

5.9.2 1T1R

A working 1T1R has been simulated, and SET/RESET/READ functions have been verified.

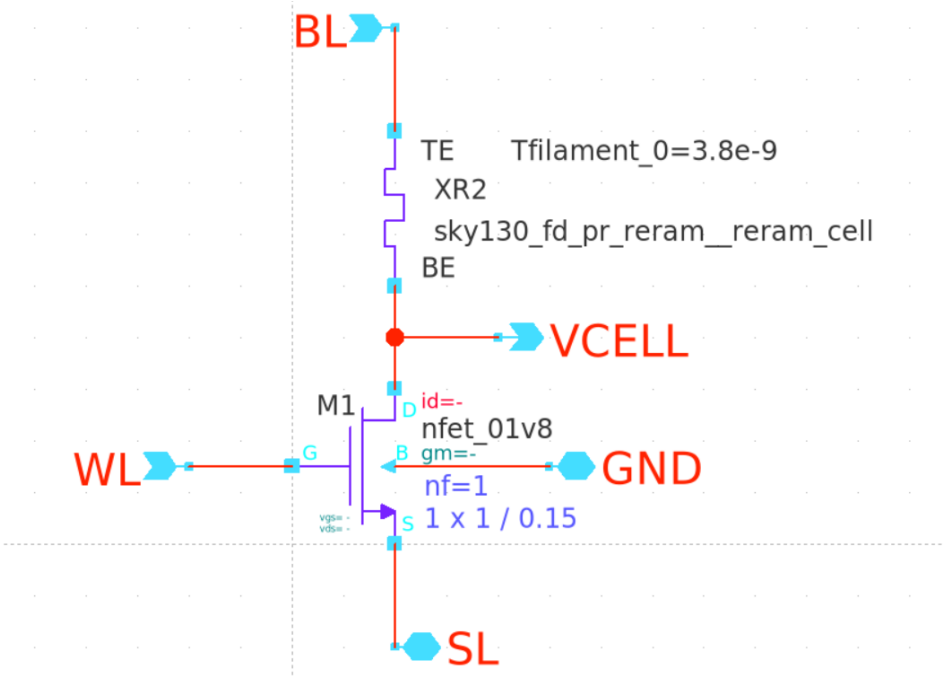


Figure 34: XSchem schematic of 1T1R

The following figure shows a 1T1R being successfully SET and RESET. The output of the simulation involving the 1T1R, the top wave is the BL (bit-line) and the bottom wave is the VD. The voltage of VD doesn't change until the value of BL reaches 2.5V, it then spikes to 1.285V, and follows the trend of BL, until BL reaches –2.5V and VD is set back to 0V. This test is crucial because it helps us understand how the ReRAM behaves, and how we should expect it to behave in our design.

With this, the resistances of the ReRAM in each respective state was calculated using Ohm's law:

- Resistance of ReRAM on SET = 9216Ω
- Resistance of ReRAM on RESET = 2.5MΩ

The results of the testbench are graphed in the figure below.

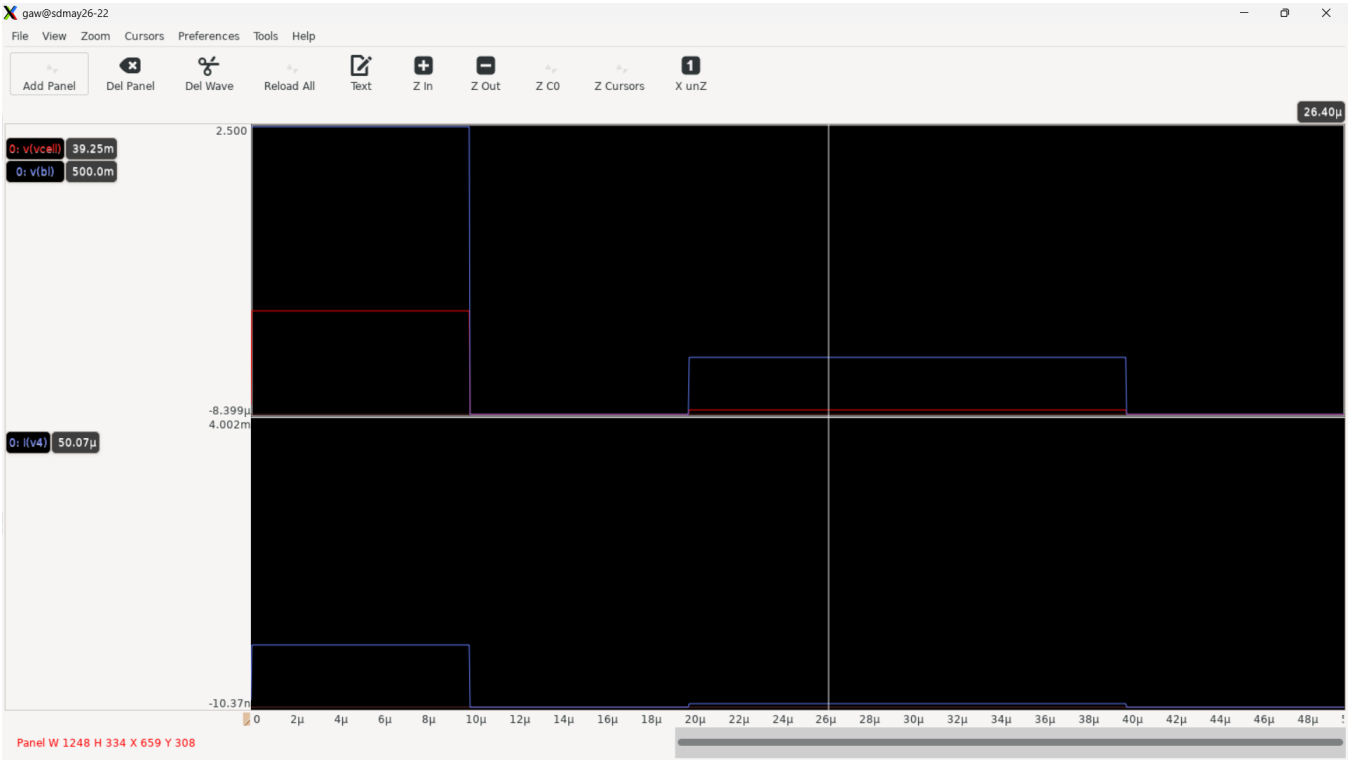


Figure 35: ReRAM characteristics after SET operation

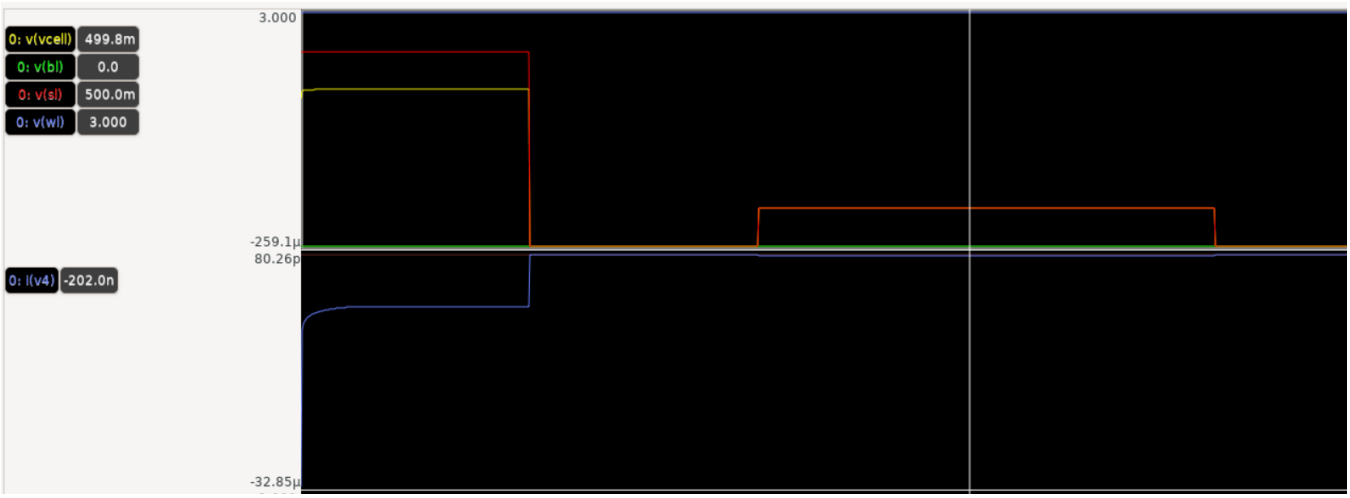


Figure 36: ReRAM characteristics after RESET operation

Below are shown waveforms produced by a correctly functioning 1T1R, where:

- BL = HIGH, SL = LOW, WL = HIGH indicates a SET
- BL = LOW, SL = HIGH, WL = HIGH indicates a RESET
- BL = $\leq$ 2.0V, SL = LOW, WL = HIGH indicates a READ

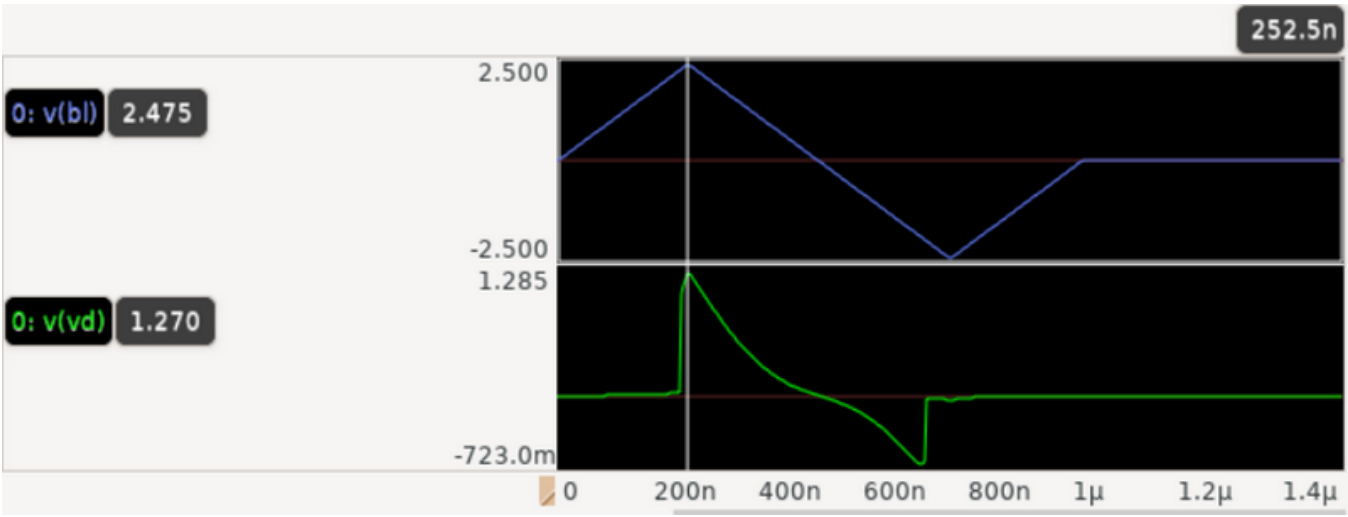


Figure 37: Simulation results of 1T1R

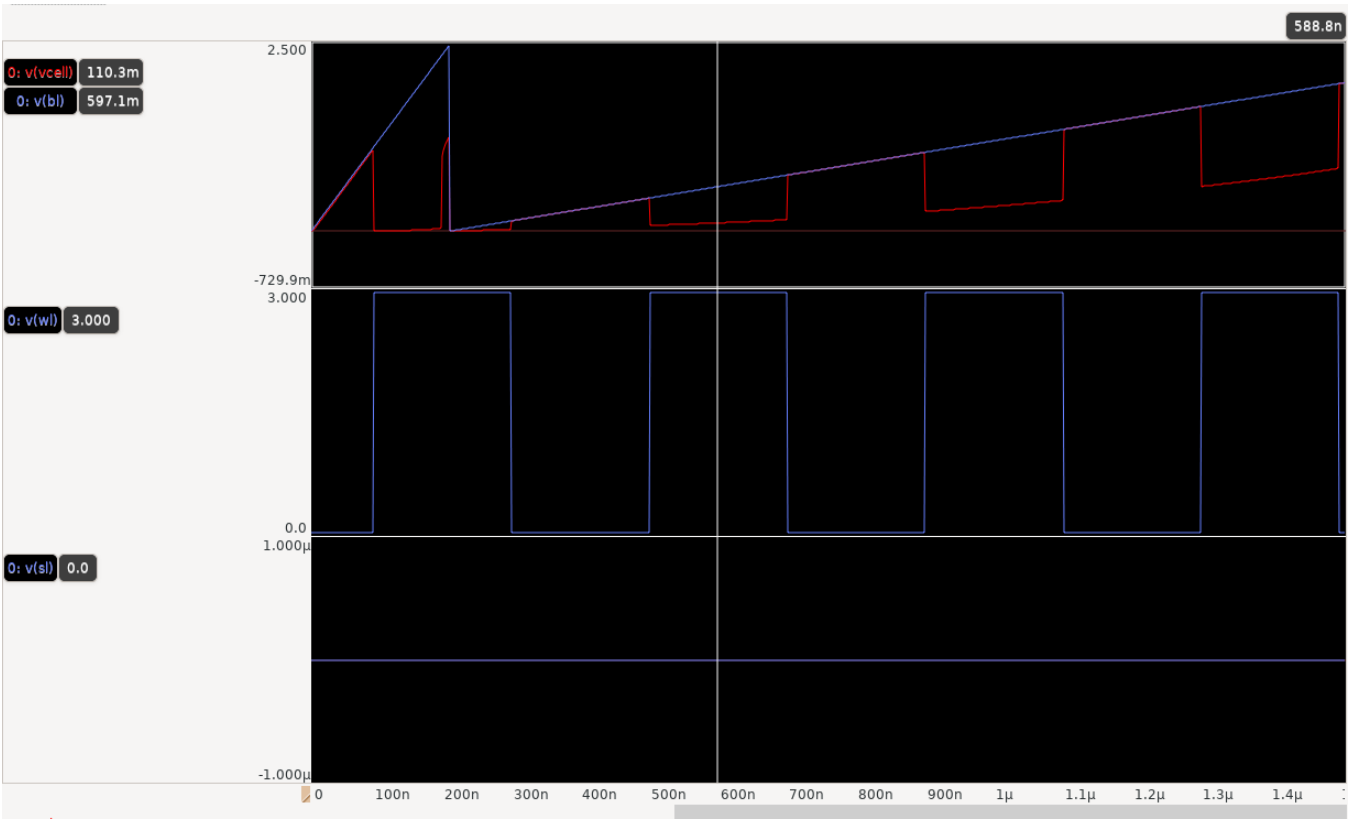


Figure 38: SET of 1T1R with WL toggle

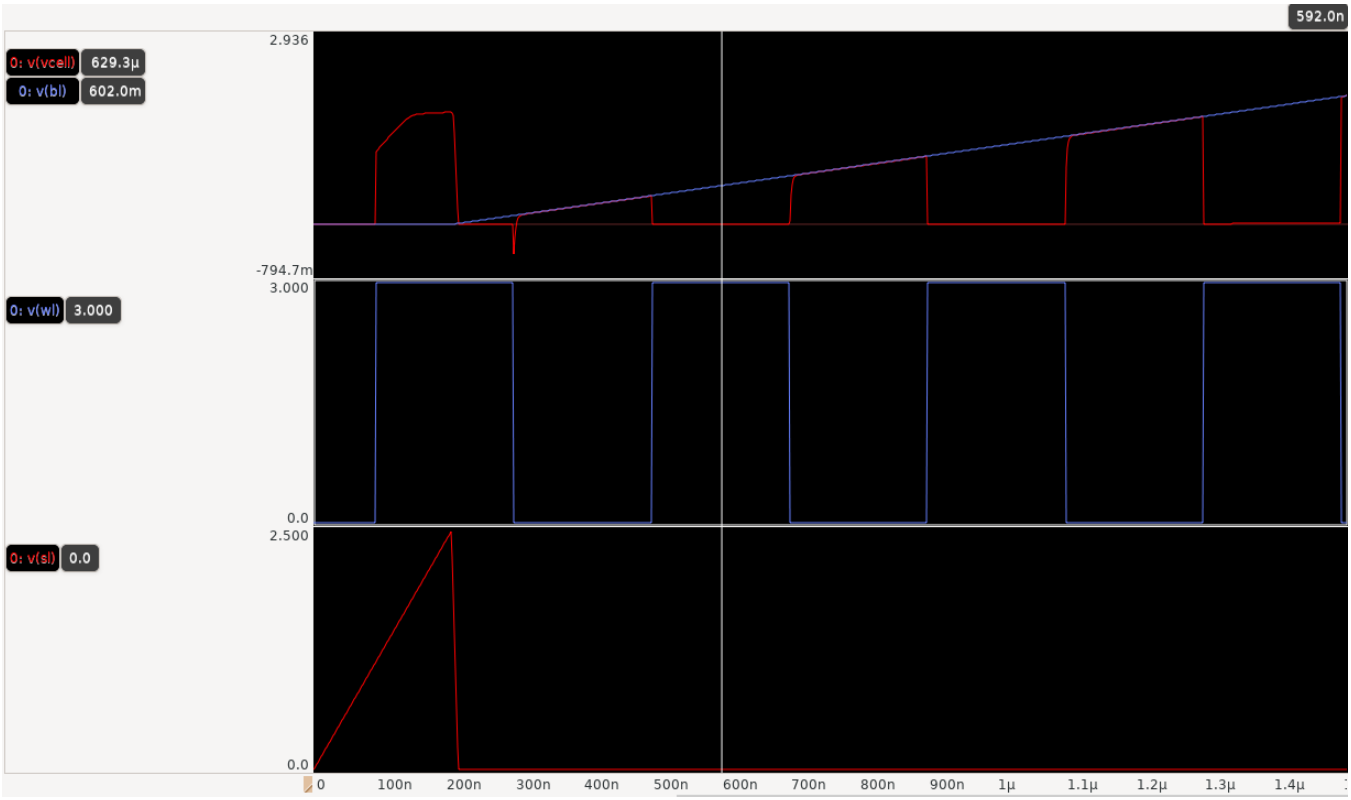


Figure 39: RESET of 1T1R with WL toggle

5.9.3 4x4 Crossbar

Using the 1T1R design, a 4x4 crossbar was created, and it was seen that each indiviudal cell can be SET/RESET and read from. A schematic is shown in the figure below. The results were verified and were seen to be accurate in a similar manner to the test of the 1T1R.

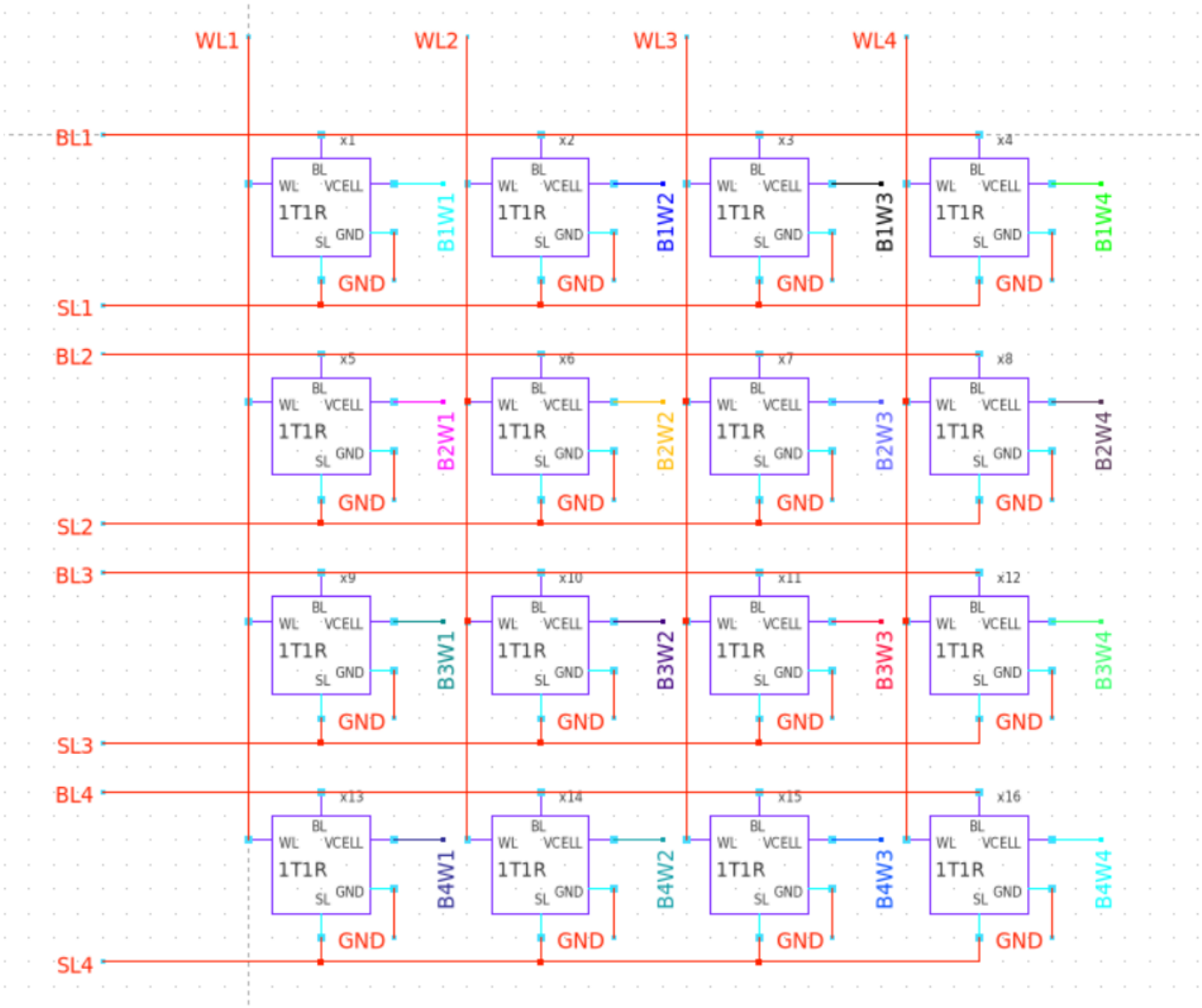


Figure 40: XSchem schematic of 4x4 crossbar

The figure below shows the results of a sample run demonstrating targeted SET and targeted RESET using wordlines and bitlines as the control. A READ operation is also demonstrated.

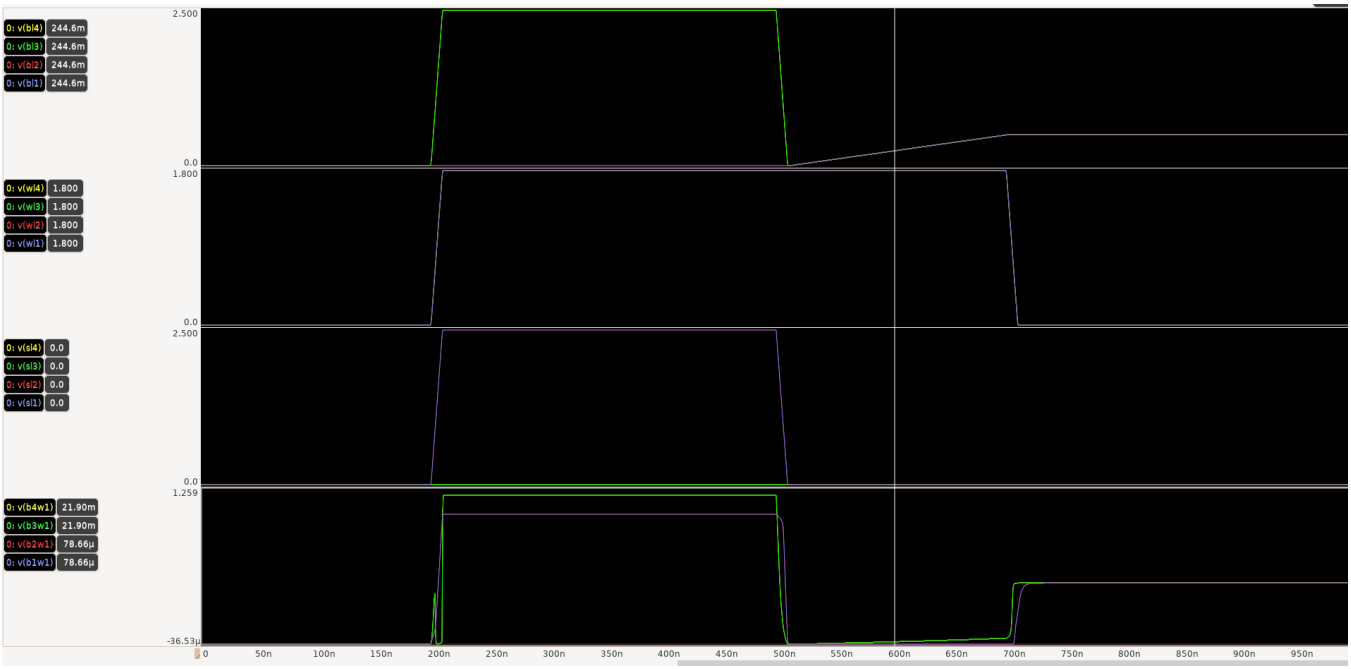


Figure 41: Simulation results of 4x4 crossbar

5.9.4 AND gate

To test the functionality of the AND gate, we tested all the possible input combinations. In the images following, it is possible to observe the inputs A & B and the output Vout. As expected the output is low while both of the inputs are not high and the output is high once both inputs are high.



Figure 42: Simulation results of a 00 input



Figure 43: Simulation results of a 01 input



Figure 44: Simulation results of a 10 input



Figure 45: Simulation results of a 11 input

5.9.5 XOR gate

To test the functionality of the XOR gate, we tested all the possible input combinations. In the images following, it is possible to observe the inputs A & B and the output Vout. As it is shown the input is only high when one of the inputs is high and the other is low, and the output is low when both inputs are the same.

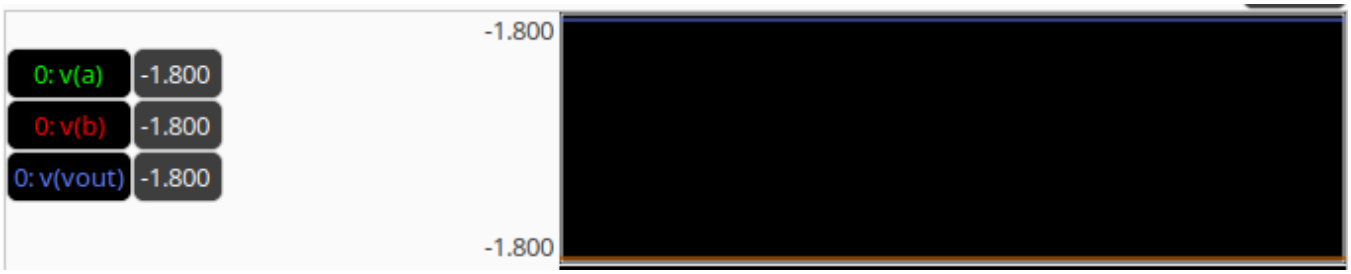


Figure 46: Simulation results of a 00 input

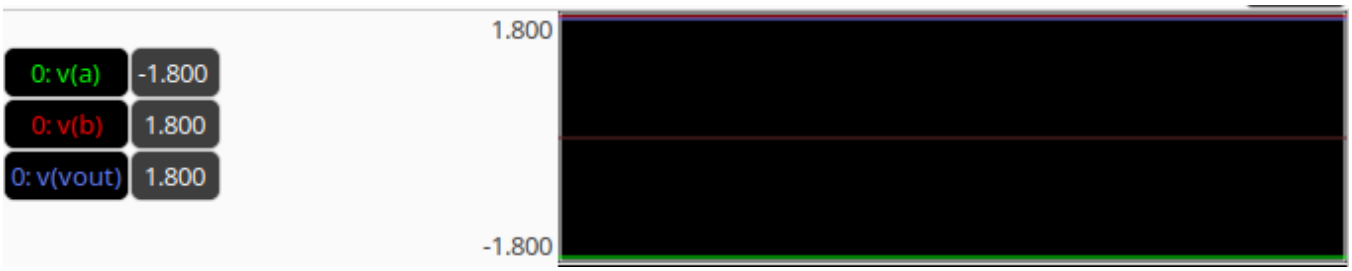


Figure 47: Simulation results of a 01 input

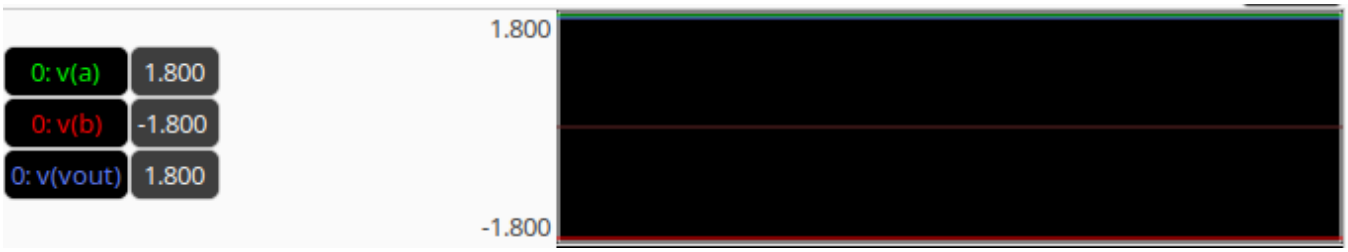


Figure 48: Simulation results of a 10 input

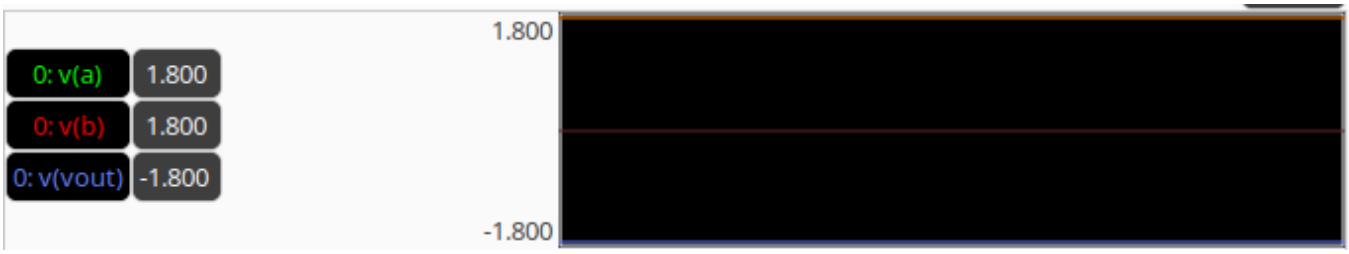


Figure 49: Simulation results of a 11 input

5.9.6 Amplifier as a Comparator

The given amplifier architectures were tested as comparators and were seen as satisfactory.

For an open-loop testbench with a sweep of noninverting input vinp, and inverting input vinm, the resulting vout is shown.

It was seen from the figure below that the comparator works as expected and has a slew rate of 55.48 $\frac{V}{\mu s}$

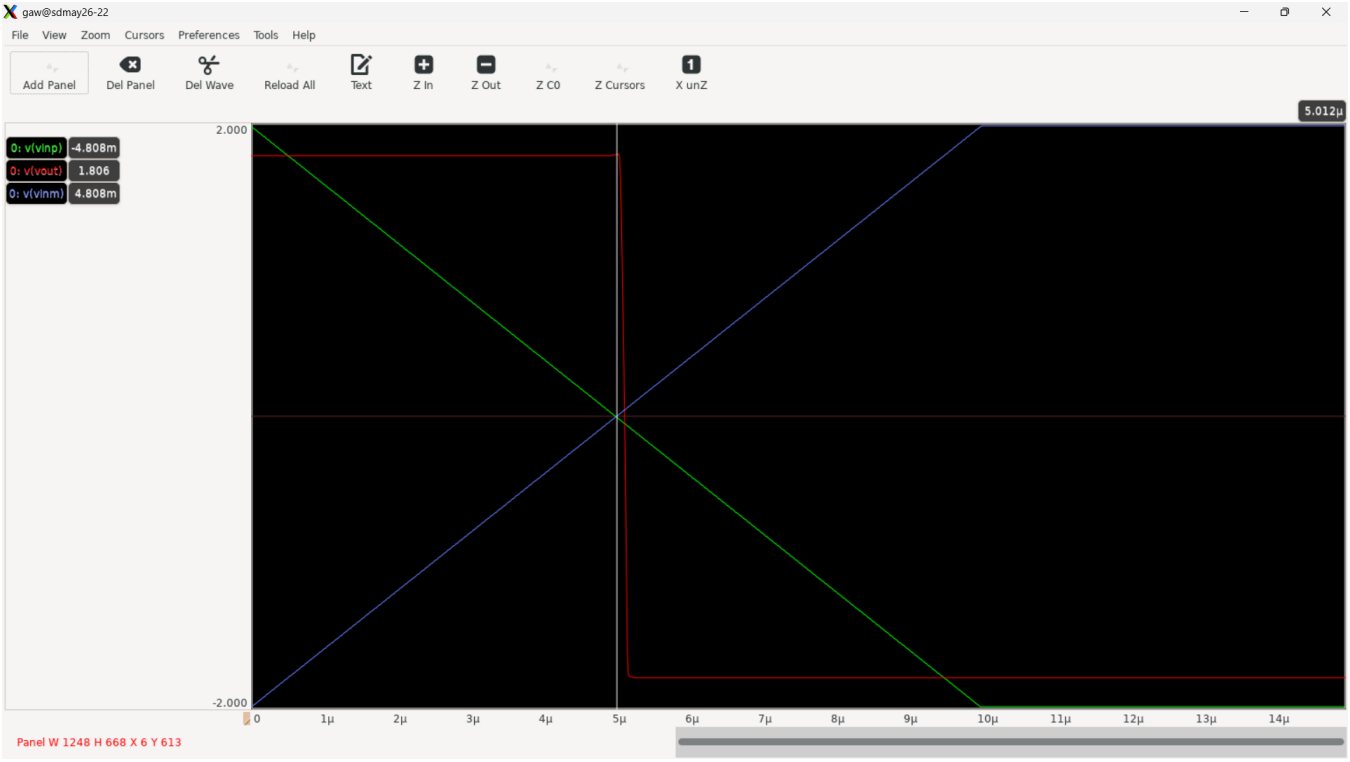


Figure 50: Comparator testing results

5.9.7 Full 1-bit compute module

The schematic of the full 1-bit compute module is provided in the figure below.

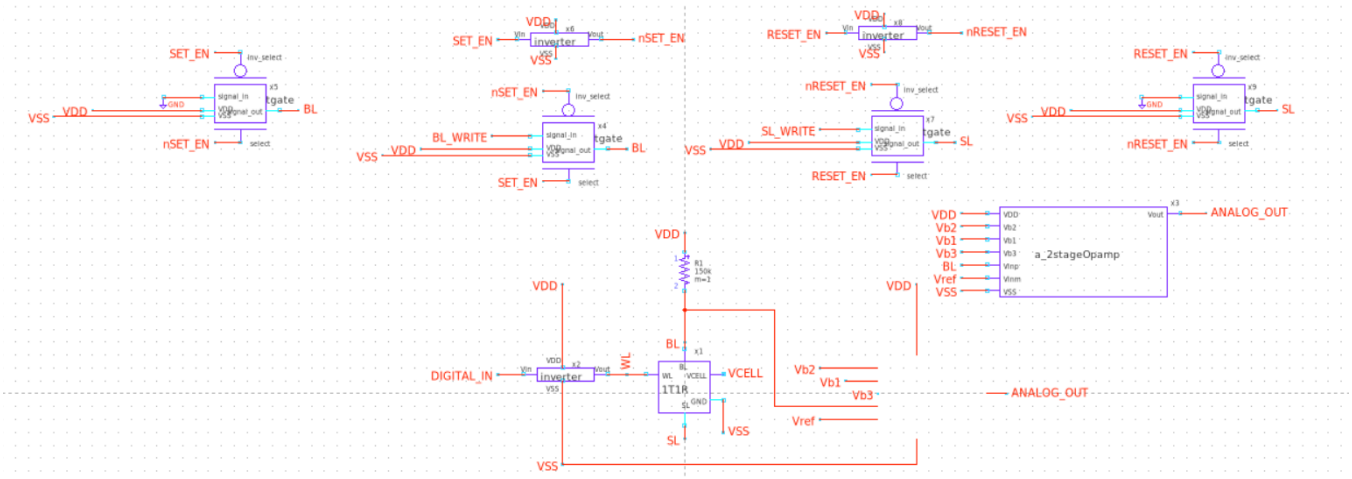


Figure 51: XSchem schematic of full 1-bit design

The following test results were validated.

- For an input of HIGH and ReRAM SET, output HIGH

- For an input of HIGH and ReRAM RESET, output LOW
- For an input of LOW and ReRAM SET, output LOW
- For an input of LOW and ReRAM RESET, output LOW

All of the above were tested, the HIGH output case is shown in the figure below.



Figure 52: Sample result for input HIGH and SET ReRAM, output HIGH

6 Professional Responsibility

6.1 Areas of Responsibility

Area of Responsibility	Definition	Relevant Items from Code of Ethics
Work Competence	Perform assigned tasks with a high level of understanding of the topics needed.	Tasks were divided within the team to best suit each member's competence within the project.
Financial Responsibility	Design and deliver products with reasonable cost and reasonable value.	Our team used open-source software to remove costs from the design stage; the only monetary expense is fabrication of the chip.
Communication Honesty	Relay honest and truthful words about the project and what has been accomplished.	Our team stays up to date through Teams and Discord about progress and future plans.
Health, Safety, Well-Being	Ensure the health and safety of the people designing and using the product.	Our team prioritizes safety of everyone involved and ensures the product has no safety problems when handled correctly.
Property Ownership	Ensure the product is defined by the client and has received verification.	We worked closely with the client, providing weekly updates and feedback on ongoing progress.
Sustainability	Ensure the product can be maintained and has reasonable longevity.	We are designing a new technology guided by client needs, affecting product longevity and maintenance.
Social Responsibility	Produce a product that benefits not only the client but also society and communities.	Our team is designing a product to further ReRAM technology and understanding of compute-in-memory systems.

Responsibility performed well: Work Competence

The team carefully assessed each member's strengths and assigned tasks to match competencies. This ensures tasks are executed effectively, contributing to a successful and functional product.

Responsibility needing improvement: Health, Safety, and Well-Being

While the team has focused on meeting requirements, proper written instructions for safe use of the product are lacking. Improvement will come from creating clear and concise usage guidelines to ensure safety and efficiency.

6.2 Project Specific Professional Responsibility Areas

Important Broader Context-Principle Pair: Environmental - Beneficence

One of the primary benefits is reducing energy consumption for AI workloads. ReRAM Compute-in-Memory reduces data movement and energy demands of matrix-vector multiplication, widely used in AI/ML applications.

Steps to ensure this pair is met:

Broader Context	Beneficence	Nonmaleficence	Respect for Autonomy	Justice
Public health, safety, and welfare	Reduces power demands in AI/ML applications, specifically for large data centers.	Avoids excessive load on power grid.	Characterization leaves design decisions to researchers and engineers.	Lower power consumption benefits all equally.
Global, cultural, and social	Open-source tools ensure design is accessible to all researchers.	Avoids alienating groups with fewer resources.	Design is reproducible and modifiable without licensing restrictions.	Equal access to design files for all groups.
Environmental	Reduces load on power grid, lowering pollution from energy generation.	Avoids environmental harm associated with power generation.	Characterization data includes power draw to help researchers choose sustainable systems.	Lower power consumption benefits all equally.
Economic	Design may reduce electricity costs via lower power consumption.	Characterizations provide insights for informed use.	Characterizations allow users to make informed decisions.	Open-source nature does not discriminate financially; however, cost reductions mainly benefit large data centers.

- Designing for lower power consumption.
- Documenting power consumption through characterization results.

Lacking Broader Context-Principle Pair: Economic - Justice

While the project is fully open-source and removes financial barriers, cost reductions from improved power efficiency disproportionately benefit large data centers.

Counterbalances to overcome the negative:

- Open-source nature ensures equal access to knowledge and tools.
- Environmental and public welfare benefits apply broadly, offsetting inequities in economic gain.

6.3 Virtues

The top three virtues demonstrated by our team are:

- Transparency - One of the main goals of our project is having the design be documented for future teams, and the most important virtue around that goal is the transparency of what we do, how we do it and the results of those actions. As a team we will be documenting all our progress and work during the weekly meetings, weekly reports, and in the Design Document.
- Perseverance - Due to the ReRAM being an almost unexplored technology, gathering information or guidance can be challenging. Using Open-Source can also be challenging as there is little to no guidance online. As a team, we will be prepared to face those challenges until the project is finished.
- Curiosity - Each of us in the team plan to be curious and try to learn more each week as the project develops.

Ali Mannan

- Perseverance has been the virtue that I have exhibited most boldly
  - This project sees us using a lot of new tools and working with technology that is new to us. Additionally, many of the tools, and specifically the PDK, are relatively poorly documented. I believe perseverance is required to be a strong virtue to any member of the team who wishes to contribute.
  - I have demonstrated perseverance by designing a complete 4x4 crossbar, completing the layout of an inverter using exclusively open-source tools, and helping my fellow teammates with the tool set-up, which was a non-trivial task.
- Curiosity is a virtue I wish to demonstrate more of
  - To be most productive and produce my best work, passion for the work itself is required. Curiosity and passion go hand-in-hand as asking questions and digging deeper is a sign of being invested in the project.
  - I can more actively participate in looking for alternative designs that our project can work on characterizing to show this virtue.

Tyler Kloser

- Throughout the project so far, the strongest virtue that I have displayed is perseverance. This project related to a new form of CIM technology that does not have many resources on so having to piece together different research articles with keeping the needs from our client has been challenging so trying to push past each roadblock and obstacle has been a struggle, but I continue the work and gain a higher understanding of our project.

- The virtue that I want to pursue more is the virtue of Curiosity. Since the project is complicated, I've had to focus on the required aspects instead of having an interest on investigating the concept further. I believe over the winter break that will give me enough time to fully process the design so far and come up with more unique ideas on how to continue with a deeper respect for the project.

Vinicius Malaman Soares

- So far this project I believe I have been able to display the virtue of perseverance. Even when tasks have felt too much or overwhelming, I have been able to stick to the work despite the obstacles. Perseverance is important when it comes to learning new things and challenging ourselves, it is proof to myself that I can stick with tasks despite their challenge.

- One virtue that is important for me and I wish to demonstrate more is curiosity. I want to start diving deeper into the project, dive deeper into Analog design, and learn more about the Analog design workflow. And more importantly, more curious about working in a team.

Austin Miller

- I believe ingenuity is the virtue I have demonstrated most clearly. Our project started with very broad, high-level goals from the client. Without a creative restructuring of these ideas into concrete engineering tasks, the team was struggling to find a starting point. I demonstrated this by synthesizing the scattered concepts from client meetings into the specific "Investigation Areas" and module lists we use now. I took the abstract goal of "characterization" and engineered the specific list of requirements (e.g., Primary vs. Tertiary goals) that gave the project its current structure.

- Focus is the virtue I wish to demonstrate more of. Up to this point, my attention has been split across the breadth of the project logistics. To ensure the design succeeds technically, I need to apply deep concentration to specific architectural challenges. I intend to shift my primary attention to the detailed implementation of our testbenches and making the working of our toolflow even easier.

7 Closing Material

7.1 Conclusion

Summary of Progress: This semester, we successfully defined the scope of our project as a "ReRAM Characterization Vehicle" and established a fully functional open-source toolchain (XSchem, Magic, NGSPICE). We have achieved two key technical milestones:

1. Reliable Simulation: We overcame significant model convergence issues to successfully simulate the SET and RESET operations of the 1T1R cell, providing the baseline expected behavior for our test structures.

2. Component Verification: We completed the layout for the 1-bit DAC (Inverter), which has passed local DRC (Design Rule Check) and LVS (Layout vs. Schematic) verification.

Current Status: Currently, our primary focus is the layout of the 1T1R (1 Transistor, 1 Resistor) cell. While the schematic simulation is functional, the layout is still in progress. We are actively resolving LVS issues related to the ReRAM cell connections to ensure the cell is manufacturable, along with discrepancies in the process laid out by ChipFoundry that are slowing down the ability to go through the full schematic to pre-check/production ready files. Until this atomic unit passes LVS, DRC and gets pushed through pre-check, we cannot proceed with other module simulation that includes parasitics.

Plan for Next Semester: Our immediate and non-negotiable priority is to finalize the 1T1R cell layout and get it to pass the Efabless (ChipFoundry) pre-check. We must verify that the parasitic extraction of this single cell does not negatively impact the SET/RESET voltages observed in our schematic simulations.

Once the 1T1R cell is fully verified, we will replicate it to build the "Process & Size Variation Array" (Module A) and the "Column Droop" structures (Module B). We will prioritize these characterization arrays over the standalone analog blocks (TIA, ADC) to ensure the client's primary goal of device characterization is met by the May 13th tapeout deadline.

7.2 References

References

[1] A. Shafiee, A. Nag, N. Muralimanohar, R. Balasubramonian, J. Strachan, M. Hu, R. S. Williams, and V. Srikumar, *ISAAC: A Convolutional Neural Network Accelerator with In-Situ Analog Arithmetic in Crossbars*, 2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA), Seoul, Korea, 2016, pp. 14-26, doi: 10.1109/ISCA.2016.12.

[2] X. Guan, S. Yu, and H.-S. P. Wong, *A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations*, IEEE Electron Device Letters, vol. 33, no. 10, pp. 1405-1407, Oct. 2012, doi: 10.1109/LED.2012.2210856.

[3] Z. Jiang, S. Yu, Y. Wu, J. H. Engel, X. Guan, and H.-S. P. Wong, *Verilog-A compact model for oxide-based resistive random access memory (RRAM)*, 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Yokohama, Japan, 2014, pp. 41-44, doi: 10.1109/SISPAD.2014.6931558.

8 Team

8.1 Team Members

- Vinicius Malaman Soares
- Austin Miller
- Ali Mannan
- Tyler Kloser

8.2 Required Skill Sets

- Schematic Design
- Testing/Simulation
- Layout
- Parasitic Extraction
- Pre-check
- C-programming

8.3 Skill Sets Covered

- **Schematic Design**: All members
- **Testing/Simulation**: All members
- **Layout**: All members
- **Parasitic Extraction**: Ali Mannan and others familiar with the process
- **Pre-check**: All members
- **C-programming**: All members

8.4 Project Management Style

We chose to adopt the Waterfall method for project management due to the dependency between different components and processes. The schematic design must be completed before moving on to testing, testing must be completed before layout, and so on.

8.5 Initial Project Management Roles

- **Vinicius Malaman Soares**: Analog Designer
- **Ali Mannan**: Analog Designer
- **Tyler Kloser**: Analog Designer
- **Austin Miller**: Analog Designer

8.6 Team Contract

Team Members:

1. Tyler Kloser
2. Ali Mannan
3. Austin Miller
4. Vinicius Malaman Soares

Team Procedures

1. **Meeting Time and Location:**
    - Face-to-face
    - Wednesdays, 2–3 PM
2. **Communication Methods:**
    - Microsoft Teams
    - Discord
3. **Decision-Making Policy:**
    - Consensus
4. **Record Keeping:**
    - Austin Miller or rotated weekly
    - Discord/Teams meeting summaries
    - Stored in Teams or CyBox

Participation Expectations

1. **Attendance and Participation:**
    - All members are expected to attend meetings on time with prior notice if absent.
    - Meeting notes will be shared for absent members.
2. **Responsibility:**
    - All members must complete tasks on time.
    - Struggles must be communicated early.
3. **Communication:**
    - At least one day notice when possible
    - Ask for help early
    - Regular progress updates
4. **Commitment:**
    - Strong effort and willingness to learn expected
    - Flexibility encouraged

Leadership

- **Team Organization**: Austin Miller
- **Client Interaction**: Tyler Kloser
- **Component Design**: Ali Mannan
- **Testing**: Vinicius Malaman Soares

Collaboration and Inclusion

Team Skills:

- **Ali Mannan**: VHDL, Verilog, Cadence Virtuoso, Embedded C, Python
- **Tyler Kloser**: VHDL, Verilog, Component Design, Software Programming
- **Austin Miller**: Cadence Tools, Analog Design, C, Python, Matlab

- **Vinicius Malaman Soares**: C, VHDL, Python, Data Analysis, Circuit Design

Encouraging Contributions:

- Open feedback
- Positive reinforcement

Conflict Resolution:

- Direct communication encouraged
- Weekly discussions if issues arise

Goals and Execution

- Functional simulated design
- Significant progress toward final implementation

Consequences

- Initial warning and support
- Advisor involvement if needed

Acknowledgment

1. Tyler Kloser Date: 09/08/2025
2. Ali Mannan Date: 09/08/2025
3. Austin Miller Date: 09/08/2025
4. Vinicius Malaman Soares Date: 09/08/2025