ReRAM ASIC Fabrication

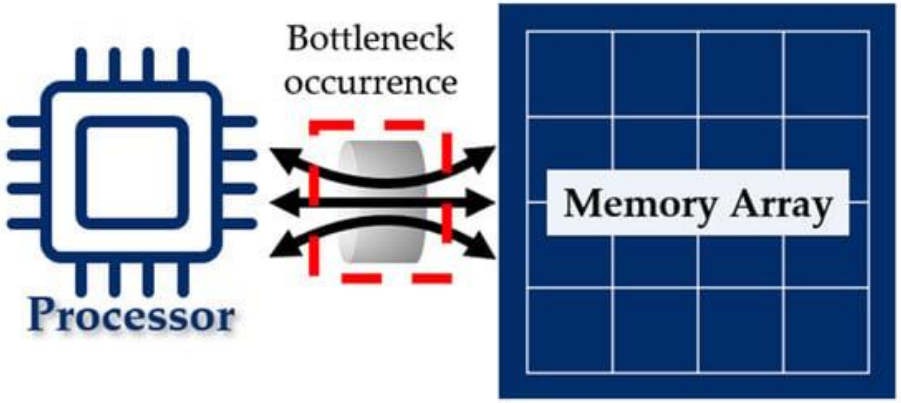
EE/CprE 4910 Design Presentation

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Problem

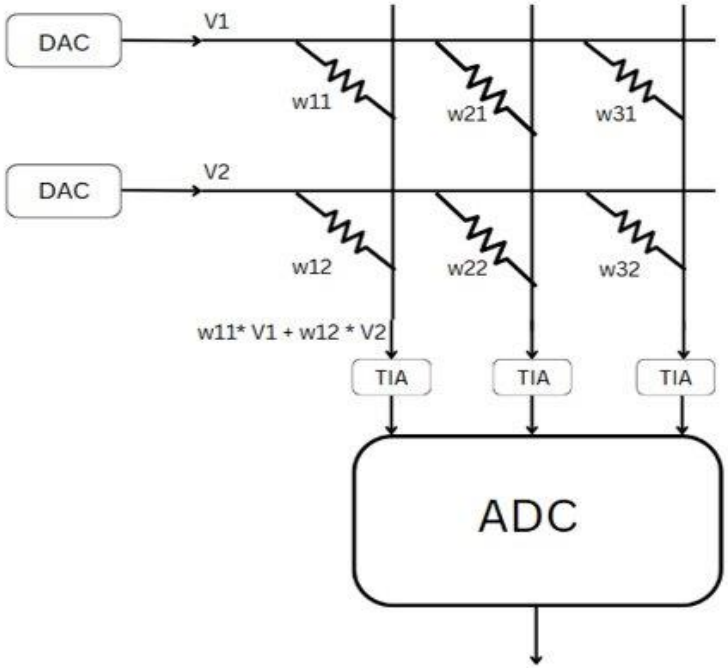
- As the AI and ML fields rapidly advance, there is more of a need for faster and more efficient computation.
- The problem is that the repeated data transfer from memory to the CPU, creates a bottleneck. This is also known von-neumann bottleneck.
- Another problem is the power wasted in this bottleneck.
- AI & ML have as the base of its computation the matrix-vector multi-plication. Requiring MAC operations.



[1]

One Possible Solution

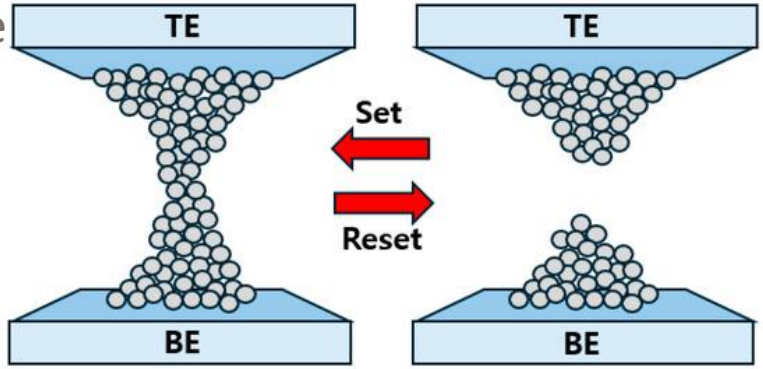
- ReRAM (Resistive Random Access Memory) can be used in a crossbar configuration to take advantage of the Analog Domain for MAC operations.
- The resulting current at each TIA is going to be the input voltage in each bit line times the resistance of each ReRAM cell.



[2]

A Little More about ReRAM

- ReRAM is a non-volatile memory
- Set and Reset operations allow for changing between Low Resistance and High Resistance states.
- LRS represents a digital 1 and a HRS represents a digital 0.



[3]

In-Memory Computing

- In-Memory computing is a great way to avoid the data transfer bottleneck. It can store the data but also perform computations
- It also offers the benefit of reducing unnecessary power consumption.
- One main problem is that ReRAM is still in its early stages, which leads to unreliable models
- There is no commercially available Resistive Random-Access Memory Devices in the market.
- Problems arise with in-memory compute technology, such as the noise and the area.

Our Goal

- The client needs a test-vehicle, for them to be able to perform their research about the behavior of ReRAM.
- We want to design and implement designs, to enable the characterization of the behaviors of the ReRAM.
- The whole design process, code, schematics and layouts are going to be made open-source
- Our final goal is that by making this project open-source and well documented we can enable researchers to understand more about ReRAM and encourage others to start learning about ReRAM

Requirements and Constraints

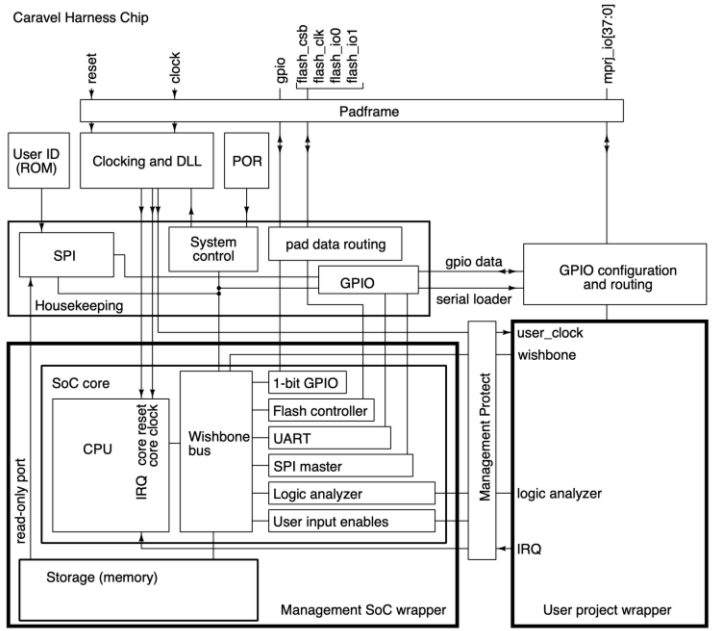
- **Requirements** split into 3 sections:
  - **Primary – Fundamental Module behavior:**
    - Tuning Curves, Endurance
    - IR Drop Due to Word and Bit Lines
    - Mixed-Signal Blocks
  - **Secondary – On Chip Interfacing:**
    - Internal Digital Control
    - IR Drop Compensation
  - **Tertiary – Compute Crossbar, Thermal Behavior:**
    - 2x2, 4x4 Crossbar
    - Internal Temp Sensor and Heater
- **Constraints** Split into Hardware and Software:
  - **Hardware:**
    - Number of Pins
    - Voltage Supplies
    - Devices Available
    - Tapeout Date of May 13th
  - **Software:**
    - Open-Source Tool Flow

Hardware Constraints

- Caravel Harness Provides Limited a Number of I/O Pins (38 Total)
- Must Use “Logic Analyzer” Pins (128 Total)
  - Used as Internal I/O to Interface with Embedded RISC-V MCU
- Voltage Ratings

Type	minimum	typical	maximum	units
Supply voltage (VDDIO)	1.8	3.3	5.0	V
Core digital supply voltage (VCCD)	1.62	1.8	1.98	V
Junction temperature	-40	27	100	$^{\circ}C$
V_{OH}	$0.8 \cdot VDDIO$		V	
V_{OL}			0.4	V

[8]



[7]

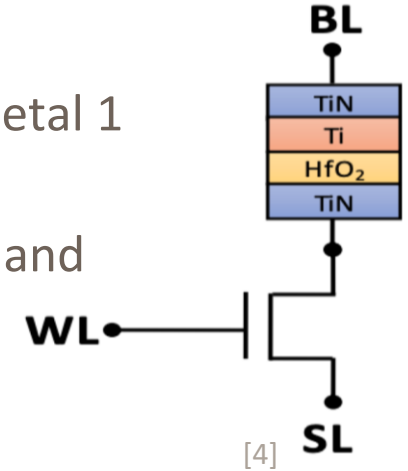
Software Constraints

- Chipfoundry Tool Flow Documentation is less than Ideal
- Unable To Simulate ReRAM Forming Process in Xschem Due to Spice Models

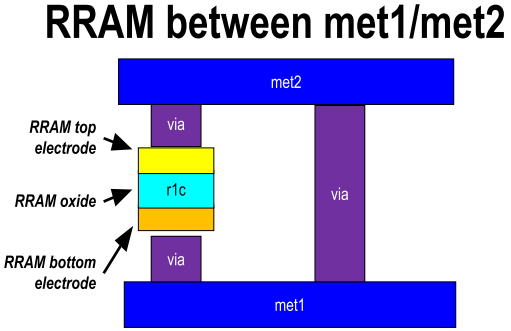


Fundamental Module

- The Most Basic Module Necessary for a Crossbar is the 1T1R
- ReRAM is 3 Layers and Sits Between Metal 1 and Metal 2
- Allows for Forming, Setting, Resetting, and Reading of the ReRAM Cell



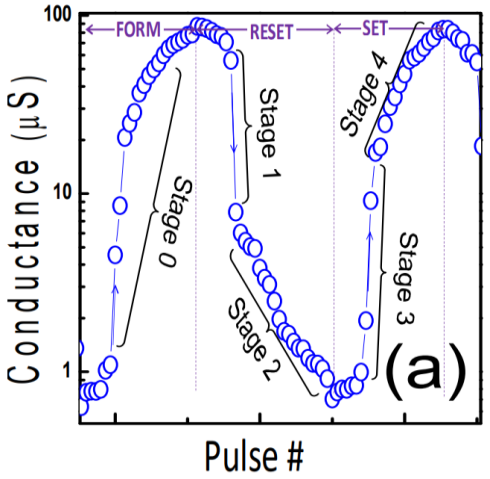
[4]



[5]

Primary Requirements

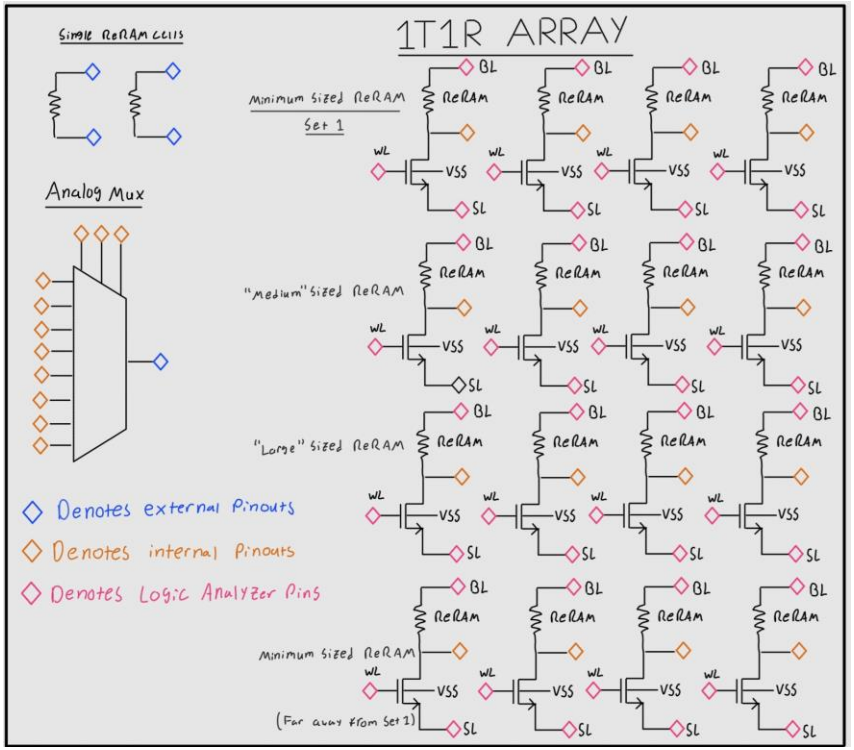
- Non-Negotiable Modules to Characterize Behavior
- **Device Physics:**
  - Generate Tuning Curves to Identify Optimal Voltages, Pulse Widths, # of Pulses
- **Endurance:**
  - Cycles to Failure and Resistance Changes
- **Variability:**
  - Device-to-Device Variation in Silicon
- **Scalability:**
  - IR Drop (Voltage Droop) When Modules are Combined



[6]

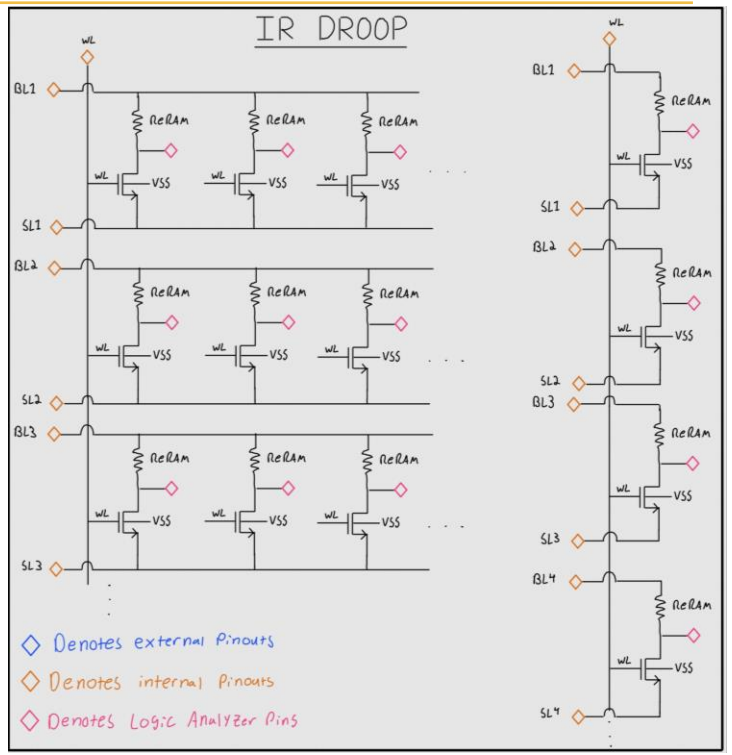
Primary Requirement Modules

- Proposed Module for Fundamental Characterizations
- Allows for:
  - **Device Physics**
    - Identify Optimal Sizing, Voltages
  - **Endurance**
    - Perform Many Set/Reset Operations on Devices of Choice
  - **Variability Tests**
    - Varied ReRAM Pillar Sizes
    - Distant Cells of the Same Size



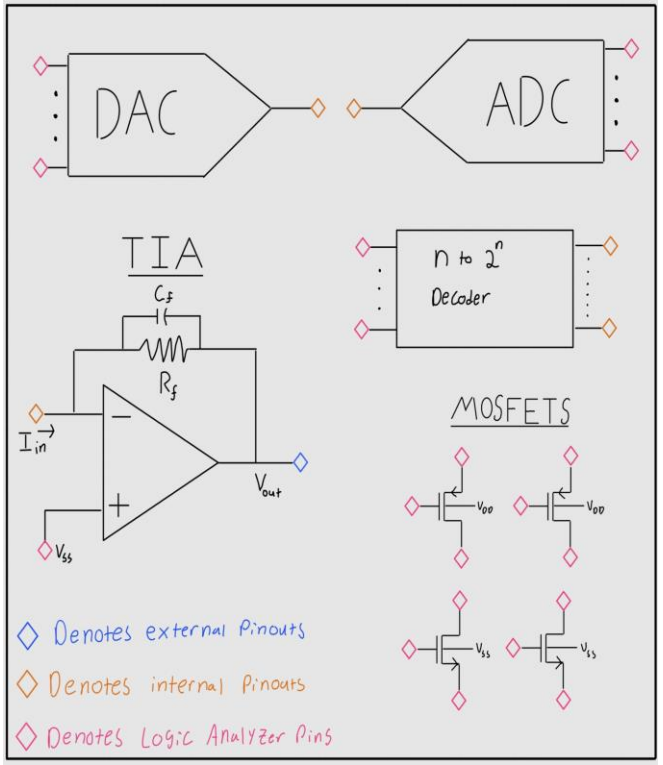
Primary Requirement Modules Cont.

- Proposed Modules for Droop Characterizations
  - Droop Can Affect the Current
  - Measure Voltage Change at Input of Bit and Source Lines
  - Measure Linearity of Current Through Bit Lines with Varying Numbers of Cells Set



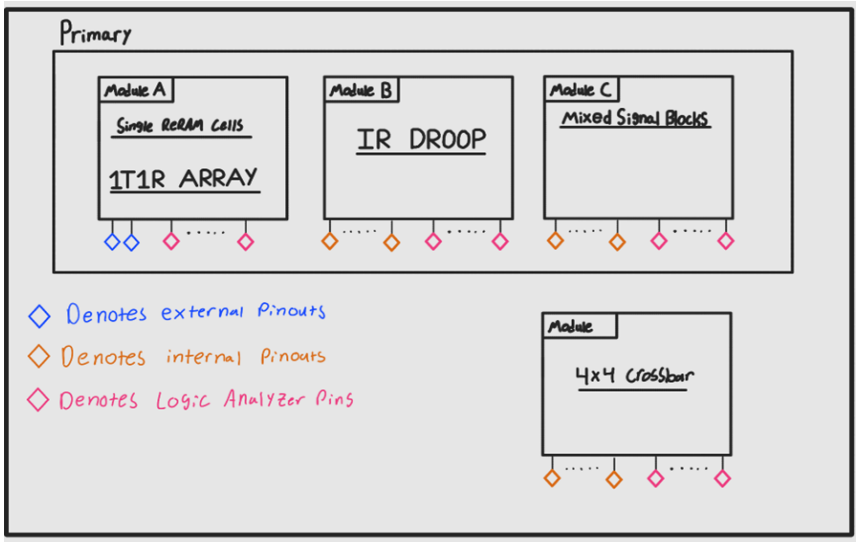
Primary Requirement Modules Cont.

- Proposed Mixed-Signal Blocks
  - Necessary to understand for Compute Crossbar
  - Pinned to Different Modules with Intermediary Pins Broken Out Between for Risk Mitigation



Secondary Requirements

- On Chip Interfacing:
  - Limited Number of I/O Pins Requires Careful Selection of Routing
  - Allow for Control and Evaluation of Nearly Every Module Through RISC-V MCU



Tertiary Requirements

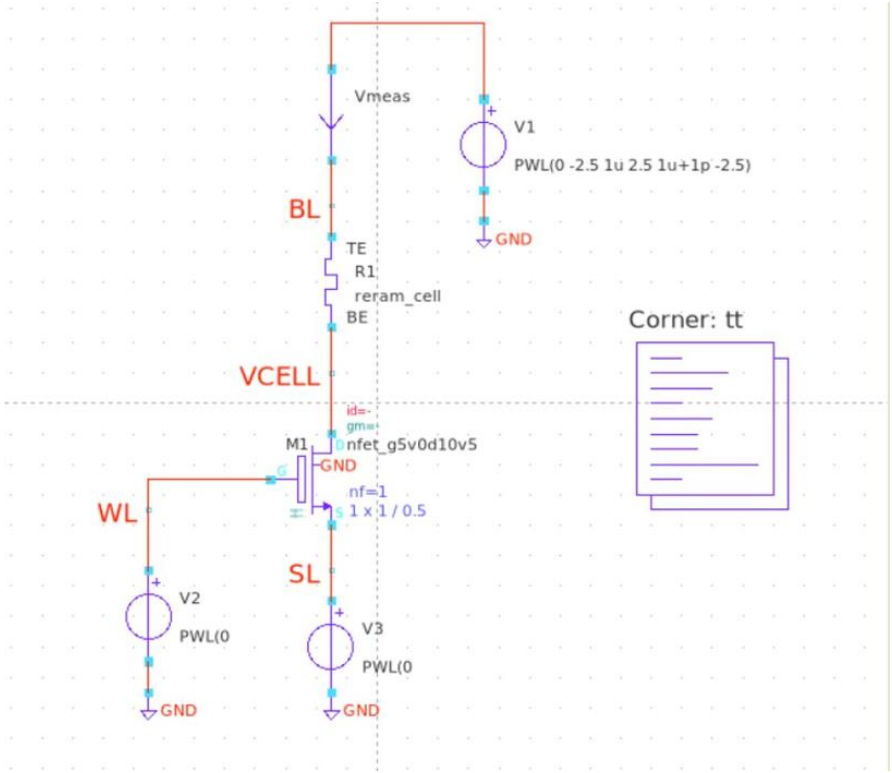
- Stretch Goals for Further Device Characterizations and Research
  - Combination of Previous Structures
    - Full Compute Crossbar (2x2, 4x4)
  - Thermal Effects
    - Thermal Noise
    - ReRAM Behavior Differences Under Different Temperatures

Design Overview and Process

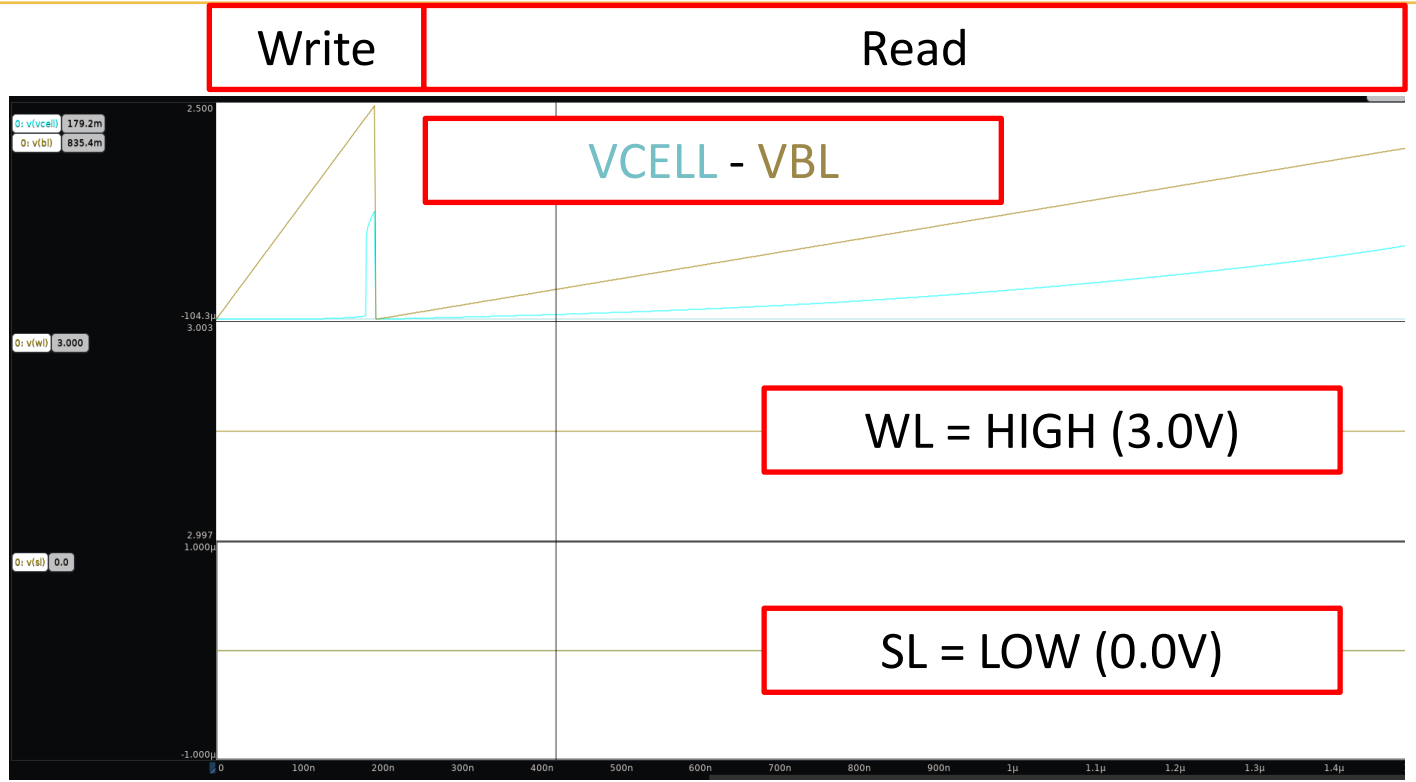
- Design flow
  - Schematic in XSchem, SPICE netlist extracted for layout
  - Testbench in XSchem, simulated with NGSPICE
  - Layout in Magic with DRC and LVS passing
  - Testbench simulation with extracted parasitics
  - Precheck

1T1R Simulations

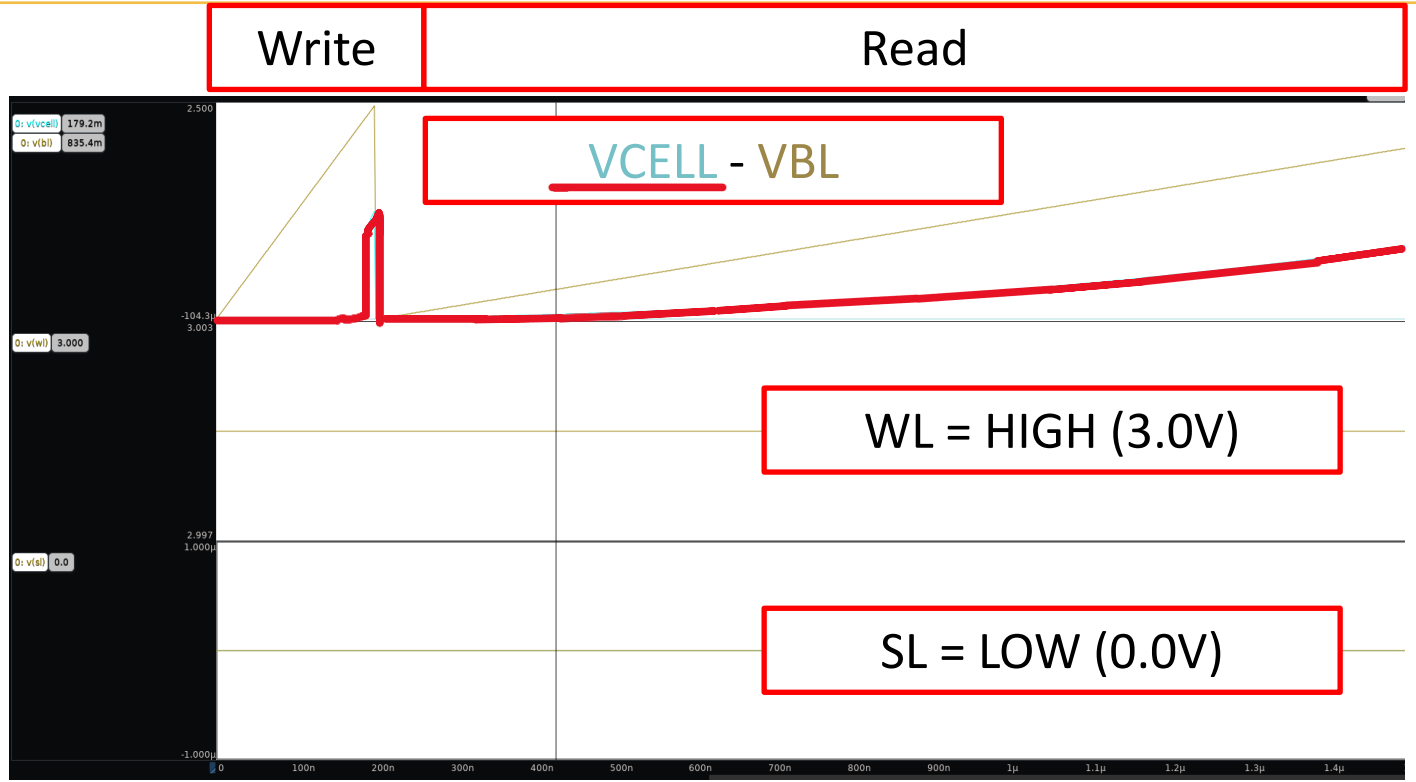
- Supports read/write with WL enable
- Writes are performed by passing a voltage through the ReRAM cell
  - SET >2.4V (low resistance)
  - RESET <-1.8V (high resistance)
- Read observes the resistance state of the cell through BL (0V, 2.0V)



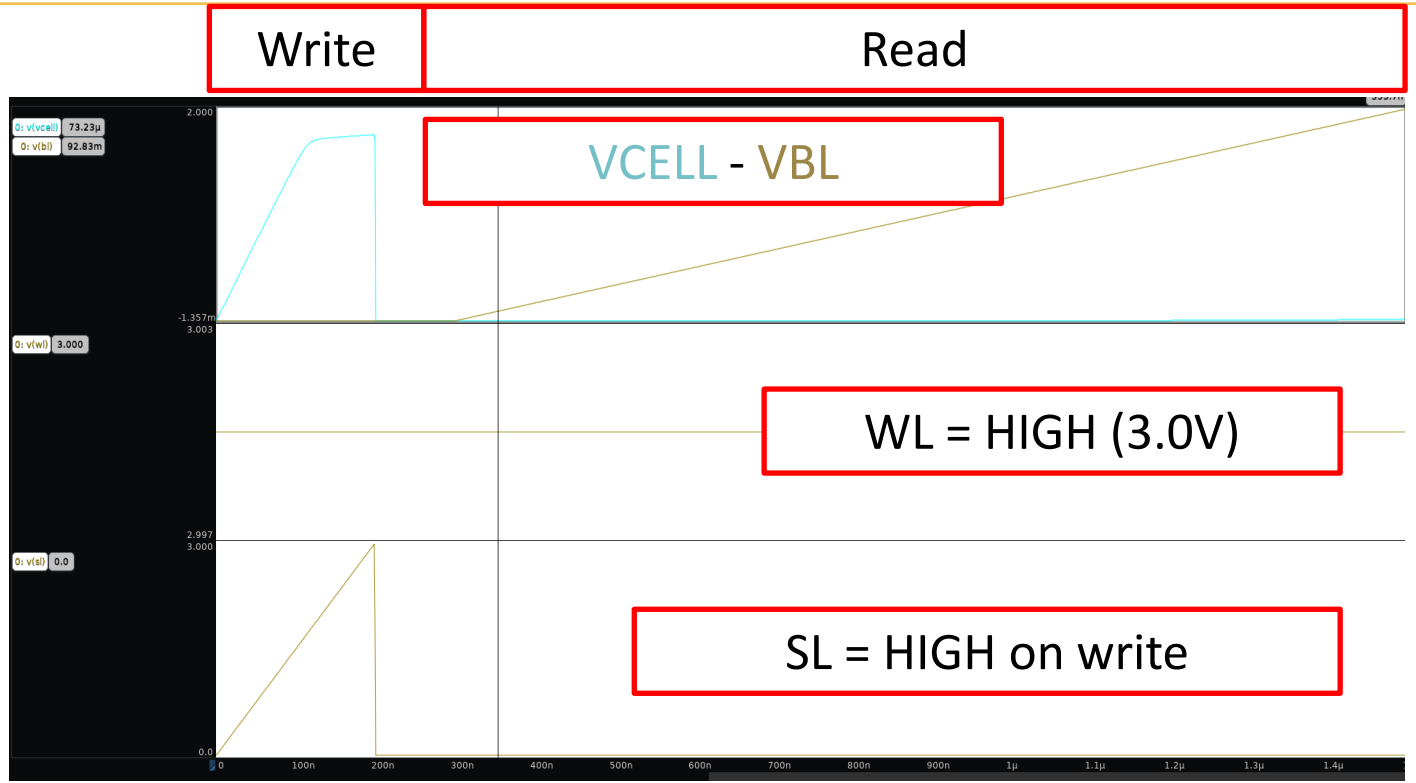
1T1R Results - SET



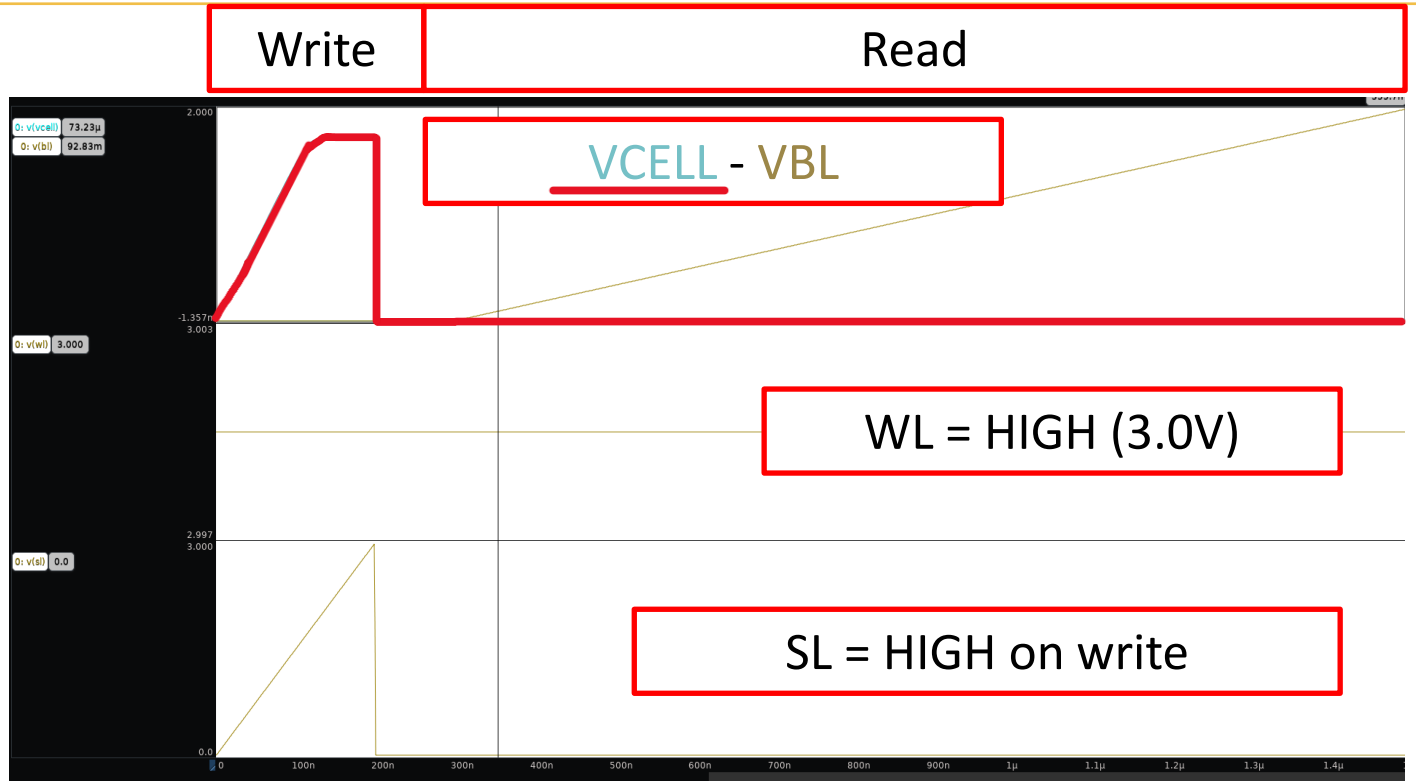
1T1R Results - SET



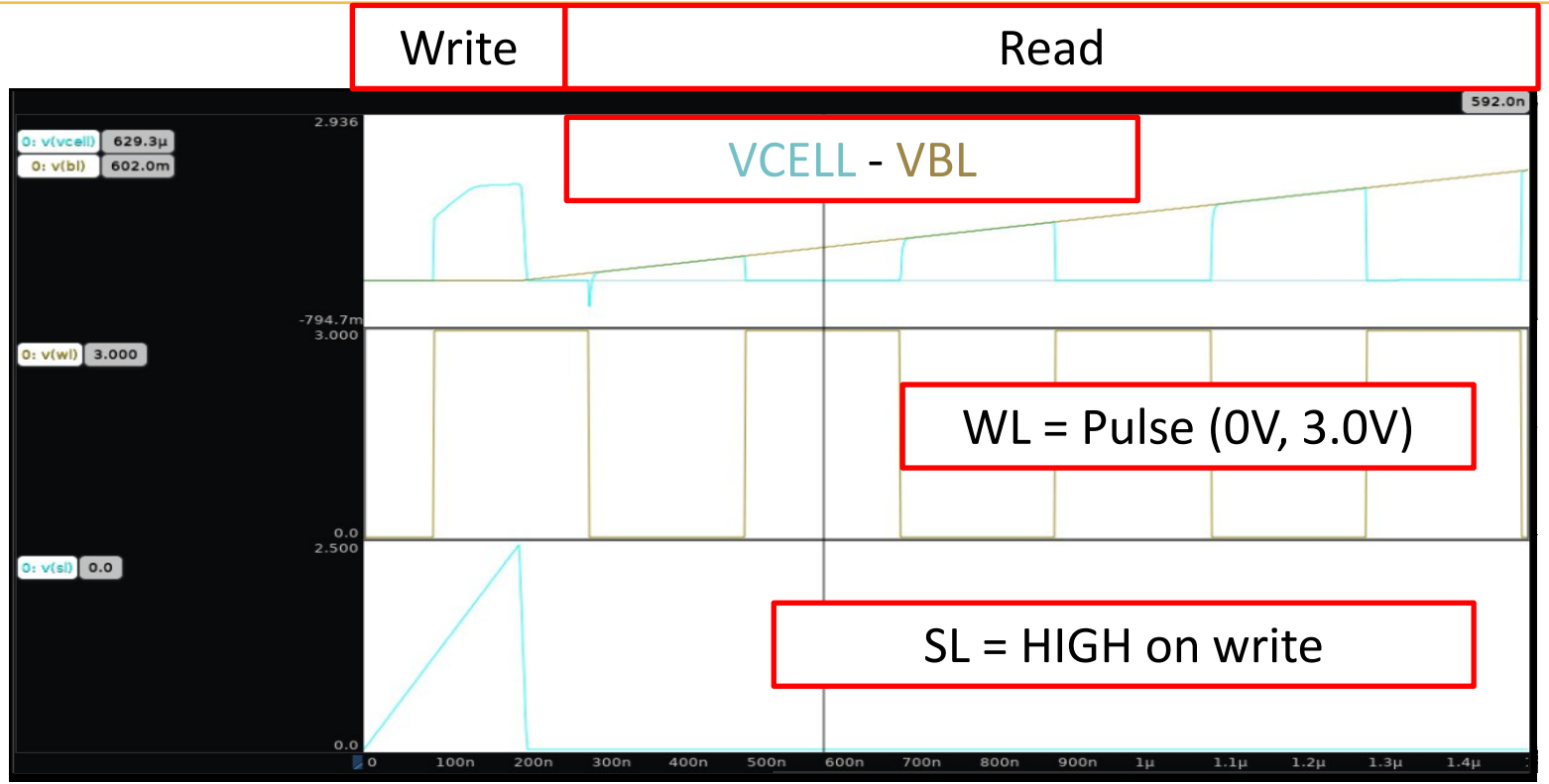
1T1R Results - RESET



1T1R Results - RESET

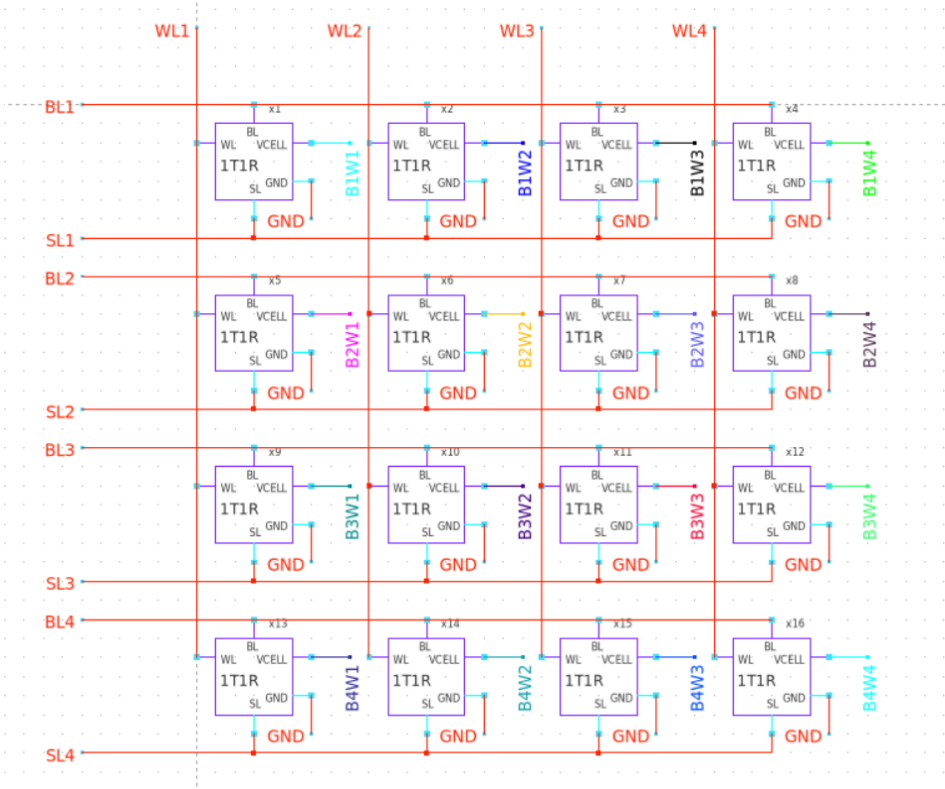


1T1R Results – RESET with WL



Crossbar Simulations

- Supports read/write operations on individual 1T1R cells
- Cell selection through a combination of BL/SL and WL



Skills Learned

- During this project we learned
  - VLSI toolflow using different open-source tools
  - ReRAM technology and practical applications
  - SkyWater 130nm design process
  - Communication within a professional environment

Semester Recap

- Tools are installed and working for all members
- 1T1R simulation
- Simulations with different crossbar setups
- 4x4 architecture

Continuing Progress (4920)

- 1T1R layout through pre-check
- Verify final characterizations the client wants
- Efabless Harness for final designs

Conclusion

- Defined the scope of our project being a characterization vehicle
- Layout, simulation, and parasitics of 1T1R
- Continue with the 1T1R to get through pre-check
- Finalize with client on wanted characterizations

References

[1] Kim Y-S, Kwon M-W. Implementation of Boolean Logic Operations and Refresh Circuit for 2T DRAM-Based PIM Architecture. Electronics. 2025; 14(22):4483. https://doi.org/10.3390/electronics14224483

[2] Made by team member Vinicius Malaman Soares

[3] Kim S, Lee J. TCAD Simulation of Resistive Switching Devices: Impact of ReRAM Configuration on Neuromorphic Computing. Nanomaterials. 2024; 14(23):1864. https://doi.org/10.3390/nano14231864

[4] E. R. Hsieh et al., “High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning,” 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 35.6.1-35.6.4, doi: 10.1109/IEDM19573.2019.8993514

[5] https://sky130-fd-pr-reram.readthedocs.io/en/latest/background.html#general-operation

[6] https://sky130-fd-pr-reram.readthedocs.io/en/latest/user_guide.html

[7] https://github.com/efabless/caravel?tab=readme-ov-file

[8] https://caravel-harness.readthedocs.io/en/latest/maximum-ratings.html